TMD2772/ TMD2772WA

Digital ALS and Proximity Module

General Description

The TMD2772/TMD2772WA family of devices provides digital ambient light sensing (ALS), a complete proximity detection system, and digital interface logic in a single 8-pin surface mount module. The devices are register-set and pin-compatible with the TMD2771 family of devices and include new and improved ALS and proximity detection features and are available with 25° and 50° fields of view. The ALS enhancements include a reduced-gain mode that extends the operating range in sunlight. Proximity detection includes improved signal-to-noise performance and more accurate factory calibration. A proximity offset register allows compensation for optical system crosstalk between the IR LED and the sensor. To prevent false proximity data measurement readings, a proximity saturation indicator bit signals that the internal analog circuitry has reached saturation.

The TMD2772/TMD2772WA ALS is based on the **ams** patented dual-diode technology that enables accurate results and approximates human eye response to light intensity under a variety of lighting conditions. The proximity detection system includes an LED driver and an IR LED, which are factory trimmed to eliminate the need for end-equipment calibration due to component variations.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of TMD2772/TMD2772WA, Digital ALS and Proximity Module are listed below:

Figure 1:
Added Value of Using TMD2772/TMD2772WA

Benefits	Features
• Minimizes board space requirements	• Ambient light sensing, proximity detection, and IR LED in a single module
• Approximates human eye response over a wide variety of lighting conditions. Achieves accurate sensing behind spectrally dark glass.	• Ambient light sensing (ALS) • Wide variety of programmable features which enable 8,000,000:1 dynamic range with very high sensitivity

Benefits	Features

• Eliminates need for customer end-product calibration.
• Reduces the proximity noise
• Control of system crosstalk and offset
• Prevents false proximity detection in bright light
• Selectable IR power-level without external resistor
• Enables wide operating range
	• Proximity detection
	  • Calibrated and trimmed to provide consistent reading
	  • Reduced proximity count variation (1)
	  • Programmable offset (1)
	  • Saturation indicator bit (1)
	  • Programmable driver for IR LED
	  • 16,000:1 dynamic range

• Reduces external processor burden	• Maskable ALS and proximity interrupt • Programmable upper and lower thresholds with persistence filter

• Enables dynamic power dissipation control	• Power management
	  • Programmable average power consumption
	  • Programmable wait time from 2.7 ms to > 8 seconds

• Industry standard two-wire interface	• I^2C fast mode compatible interface
	  • Data rates up to 400 kbit/s
	  • Input voltage levels compatible with V_{DD} or 1.8V bus

• Small foot-print module	• 3.94 mm x 2.36 mm x 1.35 mm package
• Optimize ambient light sensing angle	• Available with standard 25° (TMD2772) and wide 50° (TMD2772WA)

Note(s):

1. New or Improved feature.

Applications

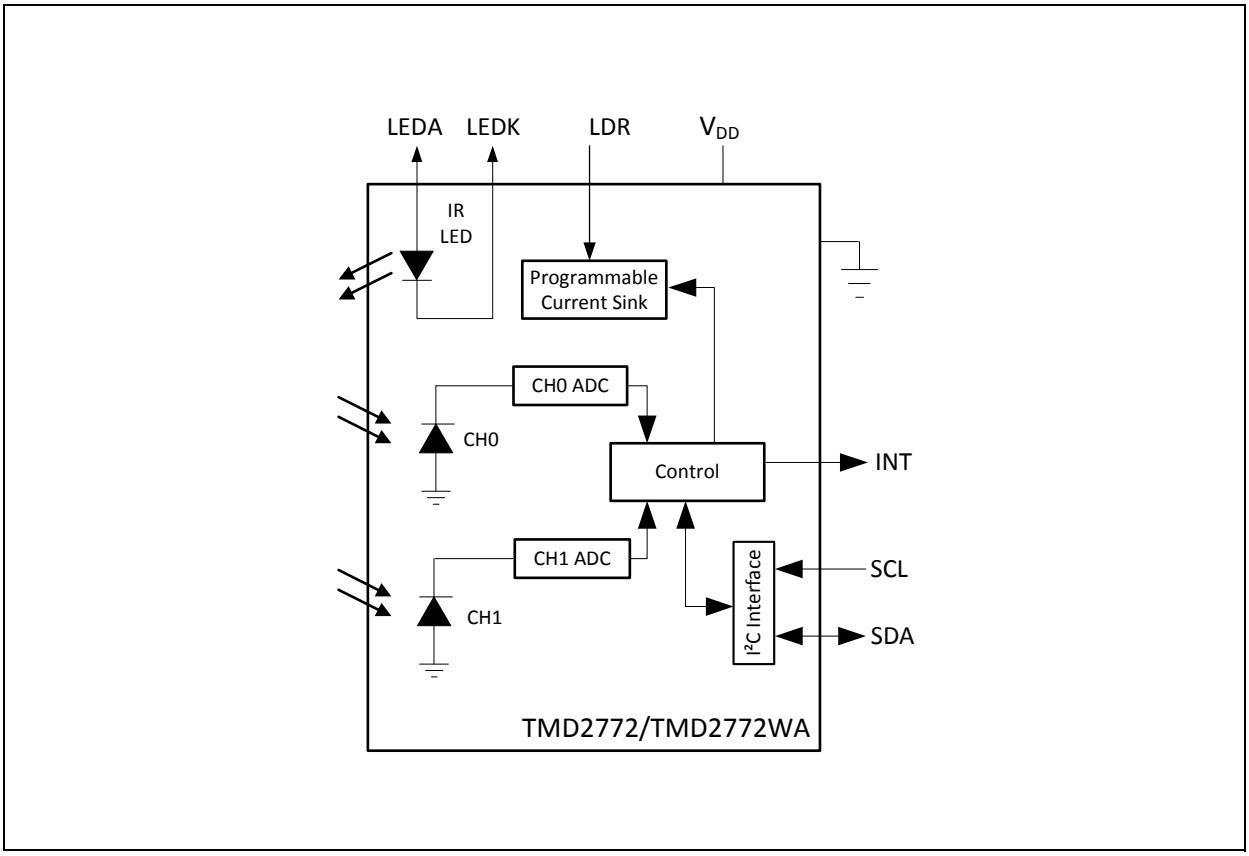
The TMD2772 applications include:

- Display Backlight Control
- Cell Phone Touch Screen Disable
- Mechanical Switch Replacement
- Industrial Process Control
- Medical Diagnostics
- Printer Paper Alignment

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
TMD2772/TMD2772WA Block Diagram



Pin Assignment

This is a Package Module - 8 pin diagram. Package drawing is not to scale.

Figure 3:
Pin Diagram (Top View)

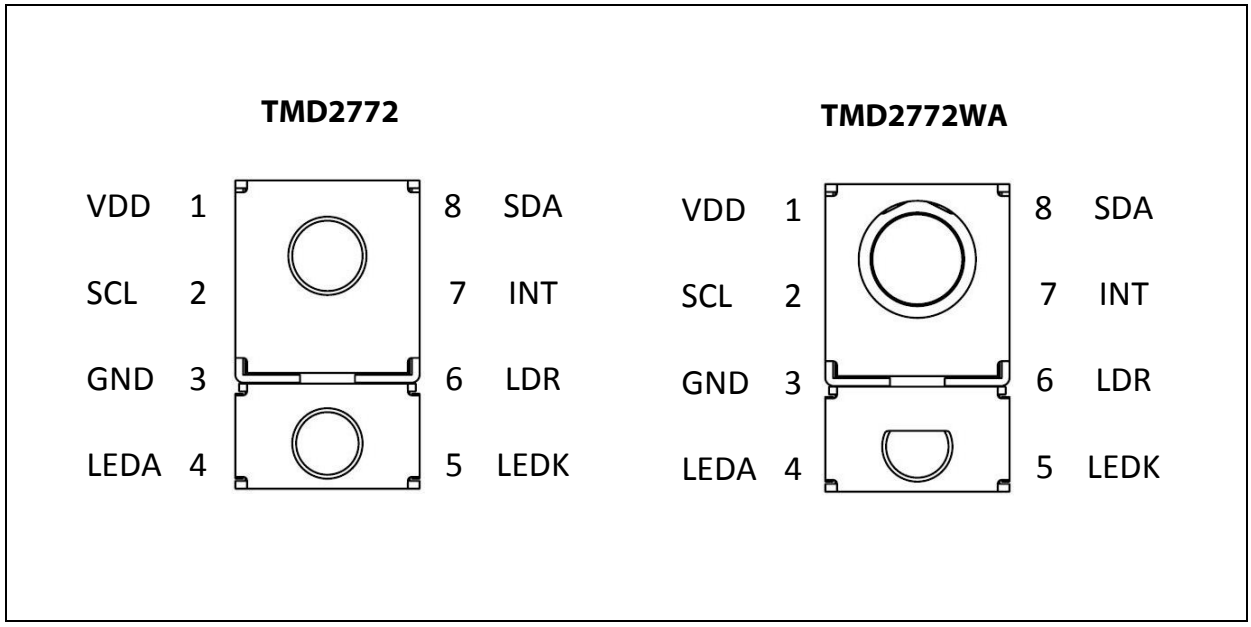


Figure 4:
Pin Description

Pin Number	Pin Name	Pin Type	Description
1	V_{DD}	Power	Supply voltage.
2	SCL	Input	I^2C serial clock input terminal — clock signal for I^2C serial data.
3	GND	Power	Power supply ground. All voltages are referenced to GND.
4	LEDA		LED anode.
5	LEDK		LED cathode. Connect to LDR pin when using internal LED driver circuit.
6	LDR		LED driver input for proximity IR LED, constant current source LED driver.
7	INT	Output	Interrupt — open drain (active low).
8	SDA	Input / Output	I^2C serial data I/O terminal — serial data I/O for I^2C.

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{DD} (1)	Supply Voltage		3.8	V
V_{LDR} (2)	Voltage on LDR signal with LDR = off. • T_A between 0° C - 70° C • T_A between -30° C - 70° C • T_A outside of -30° C - 85° C		4.8 4.6 4.4	V
V_{LEDA} (3)	LED supply voltage on LEDA input • T_A between 0° C - 70° C • T_A between -30° C - 70° C • T_A outside of -30° C - 85° C		4.8 4.6 4.4	V
V_{IO}	Digital I/O Voltage except LDR	-0.5	3.8	V
I_{Out}	Output terminal current except LDR	-1	20	mA
T_{stg}	Storage temperature range	-40	85	°C
T_A	Operating free-air temperature	-30	85	°C
I_{SCR}	Input Current (latch up immunity) JEDEC JESD78D Nov 2011	CLASS 1		µA
ESD_{HBM}	Electrostatic Discharge HBM JS-001-2014	± 2000		V
ESD_{CDM}	Electrostatic Discharge CDM JEDEC JESD22-C101F Oct 2013	± 500		V

Note(s):

1. All voltages are with respect to GND.
2. Maximum voltage with LDR = off.
3. Maximum 4.8V DC over 7 years lifetime. Maximum 5.0V spikes with up to 250s cumulative duration over 7 years lifetime. Maximum 5.5V spikes with up to 10s (=1000* 10ms) cumulative duration over 7 years lifetime.

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	2.2	3	3.6	V
	Supply voltage accuracy, V_{DD} total error including transients	-3		3	%
T_A	Operating free-air temperature (1)	-30		85	°C
V_{LEDA}	LED supply voltage on LEDA input • T_A between 0-70° C • T_A outside of 0-70° C	 2.5 2.5		 4.8 4.4	V

Note(s):

1. While the device is operational across the temperature range, functionality will vary with temperature. Specifications are stated only at 25°C unless otherwise noted.

Figure 7:
Operating Characteristics V_{DD} = 3V, T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Supply current	Active — LDR pulse off		195	250	µA
		Wait state		90		
		Sleep state — no I^2C activity		2.2	4	
V_{OL}	INT, SDA output low voltage	3 mA sink current	0		0.4	V
		6 mA sink current	0		0.6	
I_{LEAK}	Leakage current, SDA, SCL, INT pins		-5		5	µA
	Leakage current, LDR pin		-5		5	µA
V_{IH}	SCL, SDA input high voltage	TMD27721, TMD27725, TMD27721WA	0.7 V_{DD}			V
		TMD27723, TMD27727, TMD27723WA	1.25			
V_{IL}	SCL, SDA input low voltage	TMD27721, TMD27725, TMD27721WA			0.3 V_{DD}	V
		TMD27723, TMD27727, TMD27723WA			0.54	

Figure 8:
ADC Characteristics, V_{DD} = 3V, T_A = 25°C, AGAIN = 16x, AEN = 1 (unless otherwise noted)

Parameter	Test Conditions	Channel	Min	Typ	Max	Unit
Dark ADC count value	E_e = 0, AGAIN = 120×, ATIME = 0xDB (100ms)	CH0	0	1	5	counts
		CH1	0	1	5	
ADC Integration time step size	ATIME = 0xFF		2.58	2.73	2.9	ms
ADC number of integration steps			1		256	steps
ADC counts per step	ATIME = 0xFF		0		1023	counts
ADC count value	ATIME = 0xC0		0		65535	counts

Figure 9:
ALS Characteristics, V_{DD} = 3V, T_A = 25°C, AGAIN = 16x, AEN = 1 (unless otherwise noted)

Parameter	Test Conditions (1), (2), (3), (4)	Channel	Min	Typ	Max	Unit
ADC count value TMD2772 (25°)	λ_p = 625 nm, E_e = 46.8 µW/cm^2	CH0	4000	5000	6000	counts
		CH1		950		
	λ_p = 850 nm, E_e = 61.7 µW/cm^2	CH0	4000	5000	6000	counts
		CH1		2900		
ADC count value TMD2772WA (50°)	λ_p = 625 nm, E_e = 129.5 µW/cm^2	CH0	4000	5000	6000	counts
		CH1		950		
	λ_p = 850 nm, E_e = 181.2 µW/cm^2	CH0	4000	5000	6000	counts
		CH1		2900		
ADC count value ratio: CH1/CH0	λ_p = 625 nm		0.152	0.19	0.228	
	λ_p = 850 nm		0.43	0.58	0.73	
Re Irradiance responsivity TMD2772 (25°)	λ_p = 625 nm	CH0		107.2		counts /(µW/ cm^2)
		CH1		20.4		
	λ_p = 850 nm	CH0		81.5		
		CH1		47.3		
Re Irradiance responsivity TMD2772WA (50°)	λ_p = 625 nm	CH0		38.6		counts /(µW/ cm^2)
		CH1		7.3		
	λ_p = 850 nm	CH0		27.6		
		CH1		16.0		
Gain scaling, relative to 1× gain setting	AGAIN = 1× and AGL = 1			0.16		x
	AGAIN = 8× and AGL = 0		7.2	8.0	8.8	
	AGAIN = 16× and AGL = 0		14.4	16.0	17.6	
	AGAIN = 120× and AGL = 0		108	120	132	

Note(s):

1. Optical measurements are made using small-angle incident radiation from light-emitting diode optical sources. Red 625 nm and infrared 850 nm LEDs are used for final product testing for compatibility with high-volume production.
2. The 625 nm irradiance E_e is supplied by an AlInGaP light-emitting diode with the following typical characteristics: peak wavelength λ_p = 625 nm and spectral halfwidth Δ_λ½ = 20 nm.
3. The 850 nm irradiance E_e is supplied by a GaAs light-emitting diode with the following typical characteristics: peak wavelength λ_p = 850 nm and spectral halfwidth Δ_λ½ = 42 nm.
4. Unless otherwise specified, measurements are taken with ATIME= 0xF6 (27 ms).

Figure 10:
Proximity Characteristics, V_{DD} = LEDA = 3V, T_A = 25°C, P_{EN} = 1 (unless otherwise noted)

Parameter	Test Conditions	Min	Typ	Max	Units
I_{DD} Supply current	LED On		3		mA
I_{LEDA} LEDA current (1)	LED On, PDRIVE = 0		100		mA
	LED On, PDRIVE = 1		50		
	LED On, PDRIVE = 2		25		
	LED On, PDRIVE = 3		12.5		
PTIME ADC conversion steps		1		256	steps
PTIME ADC conversion time	PTIME = 0xFF (= 1 conversion step)	2.58	2.73	2.9	ms
PTIME ADC counts per step	PTIME = 0xFF (= 1 conversion step)	0		1023	counts
PPULSE LED pulses (2)		0		255	pulses
LED On LED pulse width	PPULSE = 1, PDRIVE = 0		7.3		µs
LED pulse period	PPULSE = 2, PDRIVE = 0		16.0		µs
Proximity response, no target (offset)	PPULSE = 8, PDRIVE = 0, PGAIN = 4×, (3)		100		counts
Prox count, 100mm target, TMD2772 devices (4)	73 mm × 83 mm, 90% reflective Kodak Gray Card, PGAIN = 4×, PPULSE = 8, PDRIVE = 0, PTIME = 0xFF (5)	450	520	590	counts
Prox count, 100mm target, TMD2772WA devices (4)	73 mm × 83 mm, 90% reflective Kodak Gray Card, PGAIN = 4×, PPULSE = 8, PDRIVE = 0, PTIME = 0xFF (5)	235	275	315	counts

Note(s):

1. Value is factory-adjusted to meet the Prox count specification. Considerable variation (relative to the typical value) is possible after adjustment.
2. These parameters are ensured by design and characterization and are not 100% tested.
3. Proximity offset varies with power supply characteristics and noise.
4. ILEDA is factory calibrated to achieve this specification. Offset and crosstalk directly sum with this value and is system dependent.
5. No glass or aperture above the module. Tested value is the average of 5 consecutive readings.
6. Proximity test was done using the circuit shown in Figure 12. See PCB Pad Layout for recommended application circuit.

Figure 11:
Proximity Test Circuit

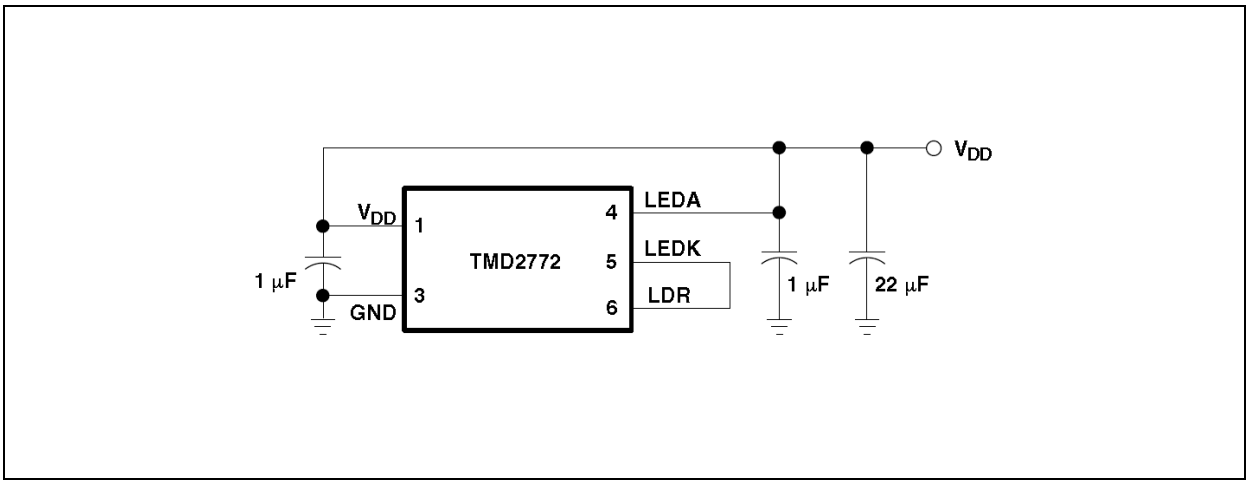


Figure 12:
IR LED Characteristics, V_{DD} = 3V, T_A = 25°C

Parameter	Test Conditions	Min	Typ	Max	Unit
V_F Forward Voltage	I_F = 100 mA	1.5		2.2	V
V_R Reverse Voltage	I_R = 10 µA	5			V
P_O Radiant Power	I_F = 20 mA	4.5			mW
λ_p Peak Wavelength	I_F = 20 mA		850		nm
Δ_λ Spectral Radiation Bandwidth	I_F = 20 mA		40		nm

Figure 13:
Wait Characteristics, V_{DD} = 3V, T_A = 25°C, WEN = 1 (unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
Wait steps		1		256	steps
Wait time	WTIME = 0xFF (= 1 wait step)		2.73	2.9	ms

Timing Characteristics

Figure 14:
AC Electrical Characteristics, V_{DD} = 3V, T_A = 25°C (unless otherwise noted)

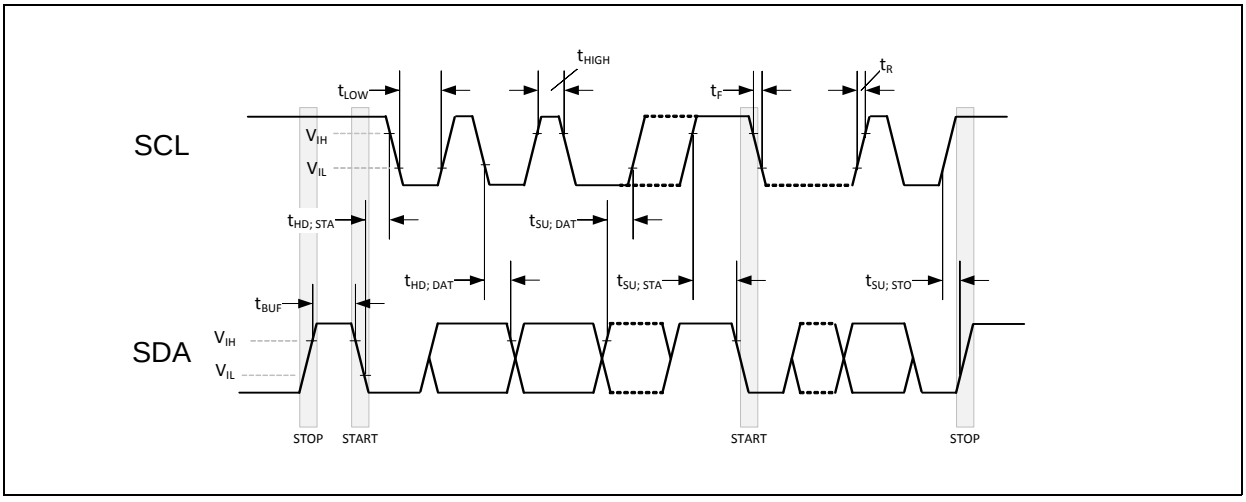
Parameter (1)	Conditions	Min	Max	Unit
f_{SCL}	Clock frequency (I^2C only)	0	400	kHz
t_{BUF}	Bus free time between start and stop condition	1.3		µs
$t_{HD;STA}$	Hold time after (repeated) start condition. After this period, the first clock is generated.	0.6		µs
$t_{SU;STA}$	Repeated start condition setup time	0.6		µs
$t_{SU;STO}$	Stop condition setup time	0.6		µs
$t_{HD;DAT}$	Data hold time	10		ns
$t_{SU;DAT}$	Data setup time	100		ns
t_{LOW}	SCL clock low period	1.3		µs
t_{HIGH}	SCL clock high period	0.6		µs
t_F	Clock/data fall time		300	ns
t_R	Clock/data rise time		300	ns
C_i	Input pin capacitance		10	pF

Note(s):

1. Specified by design and characterization; not production tested.

Timing Diagrams

Figure 15:
Parameter Measurement Information



Typical Operating Characteristics

Figure 16:
Spectral Responsivity

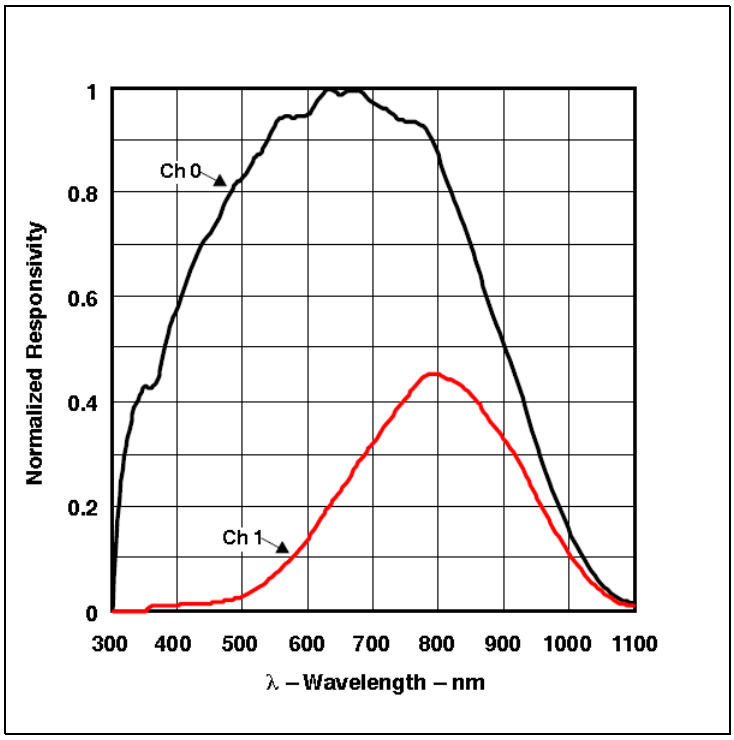


Figure 17:
Normalized I_{DD} vs. V_{DD} and Temperature

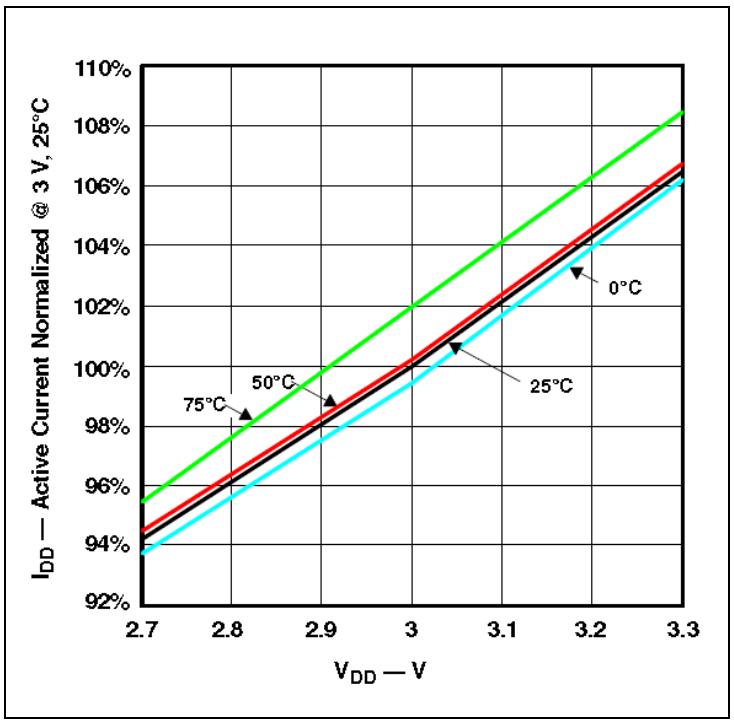


Figure 18:
Normalized Responsivity vs. Angular Displacement for Non-WA and WA Devices

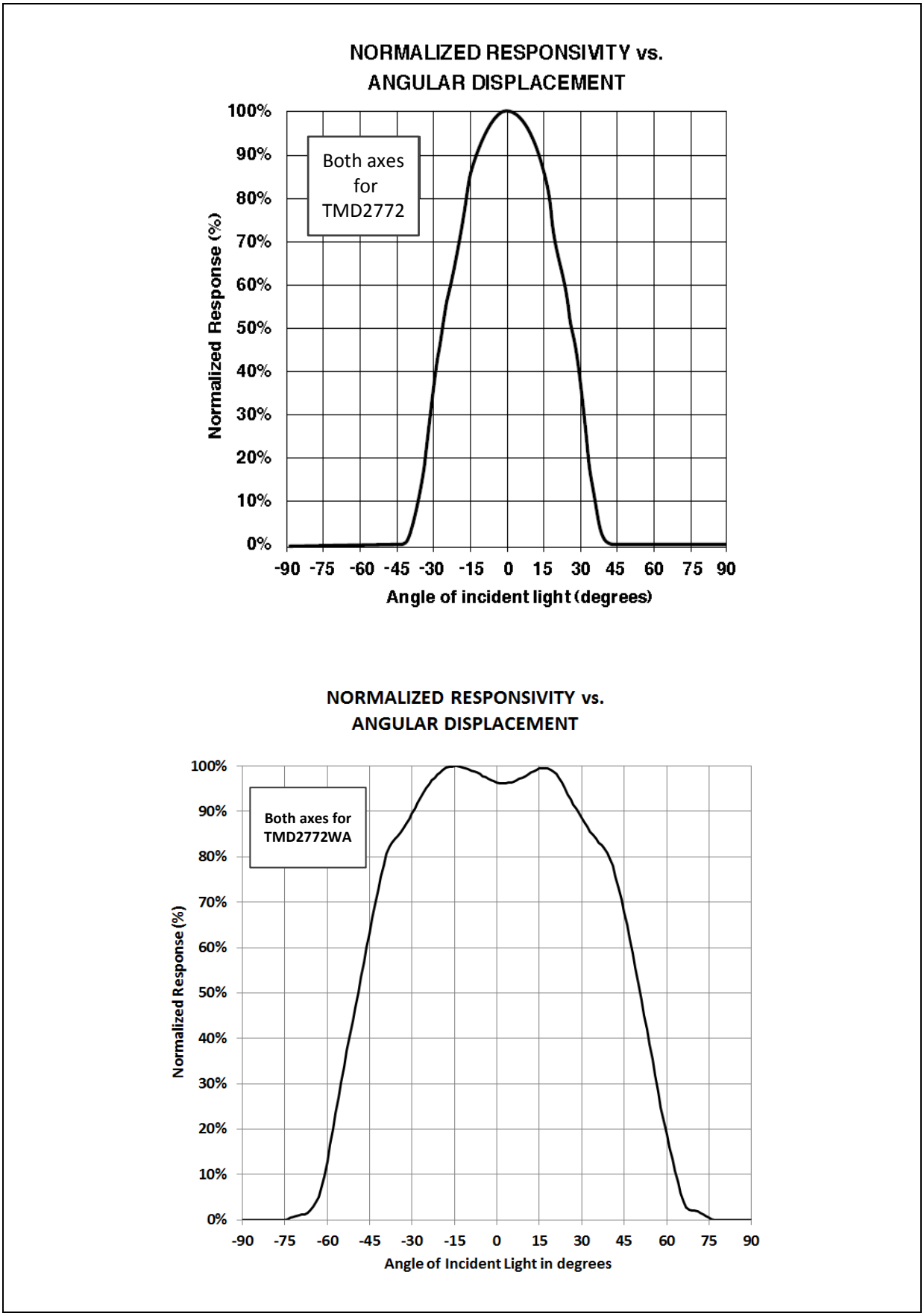


Figure 19:
Proximity Response of TMD2772 and TMD2772WA Modules

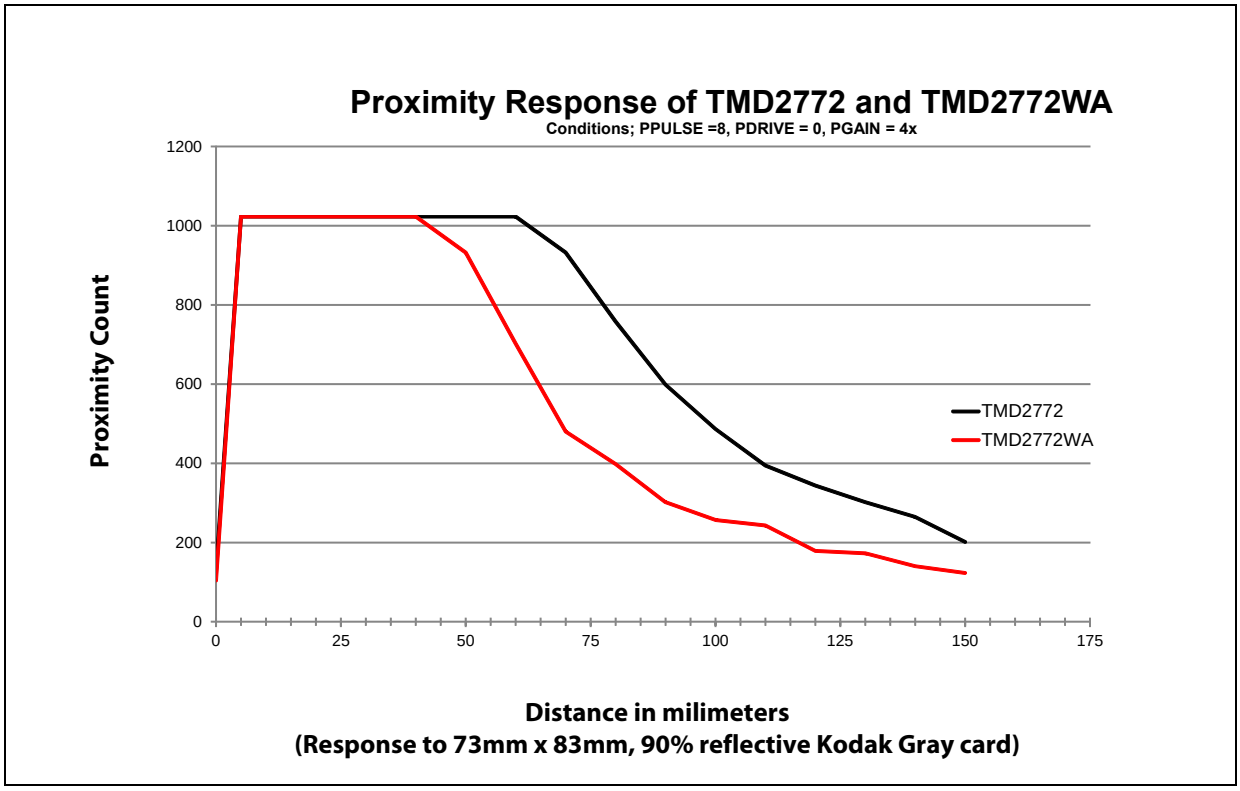
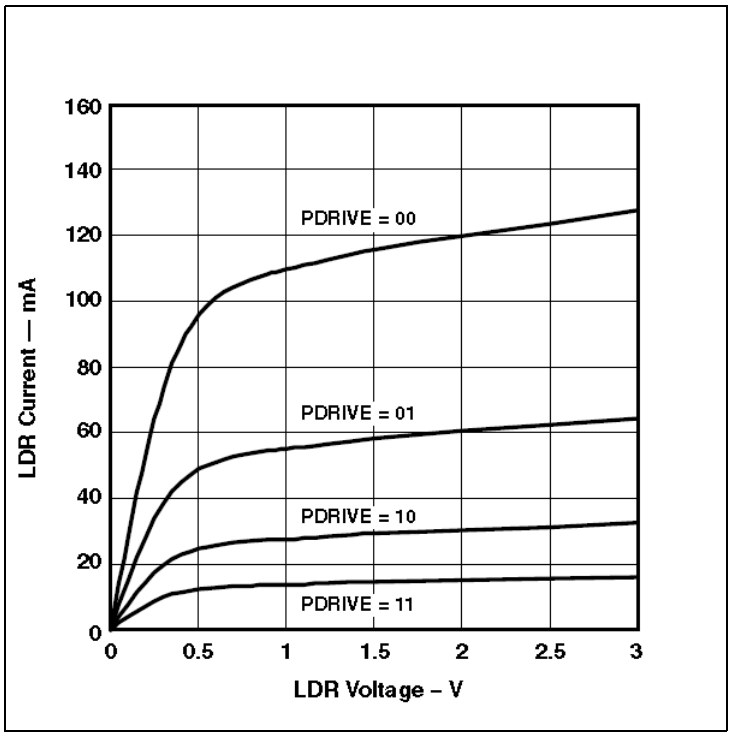


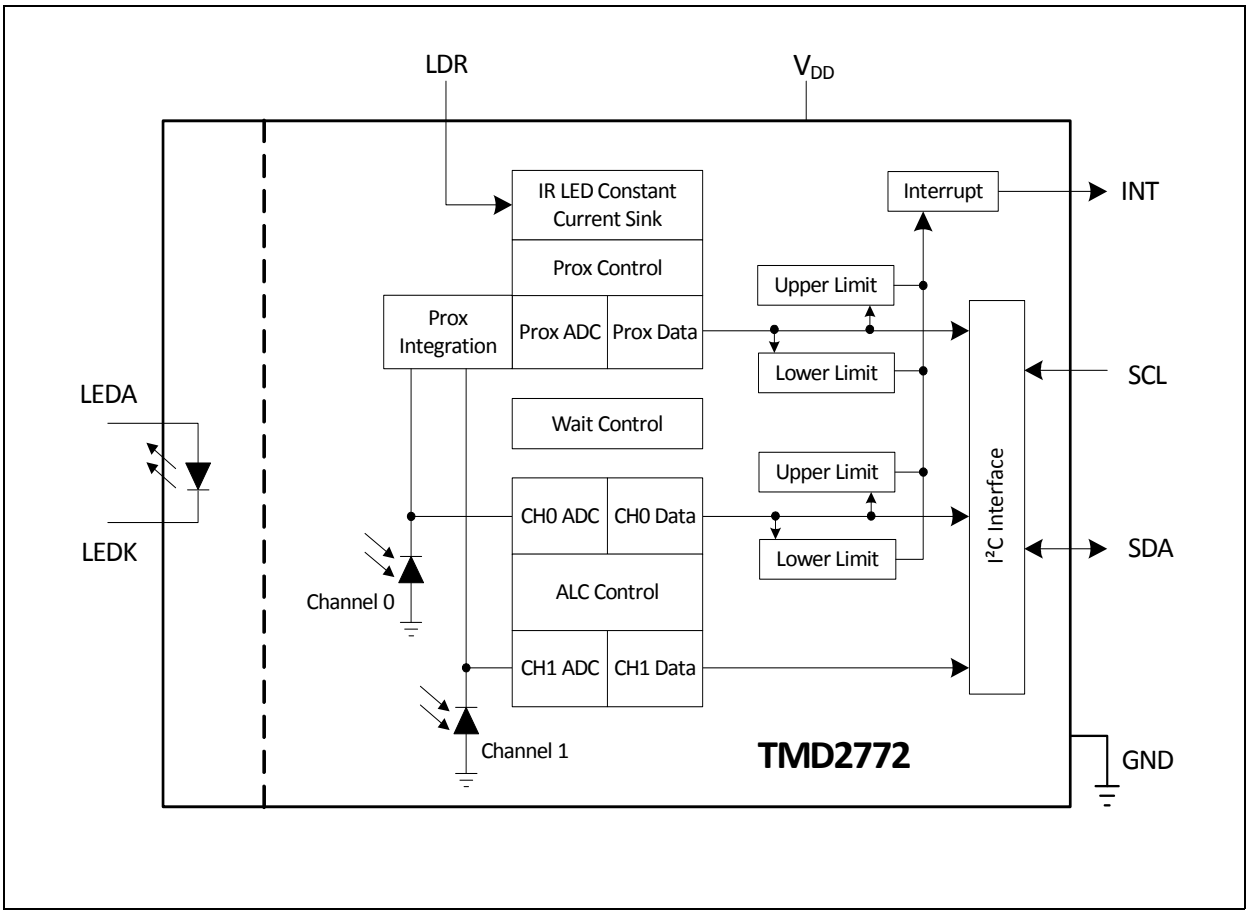
Figure 20:
Typical LDR Current vs. Voltage



Detailed Description

The light-to-digital device provides on-chip photodiodes, integrating amplifiers, ADCs, accumulators, clocks, buffers, comparators, a state machine, and an I²C interface. Each device combines one photodiode (CH0), which is responsive to both visible and infrared light, and a second photodiode (CH1), which is responsive primarily to infrared light. Two integrating ADCs simultaneously convert the amplified photodiode currents to a digital value providing up to 16-bits of resolution. Upon completion of the conversion cycle, the conversion result is transferred to the Ch0 and Ch1 data registers. This digital output can be read by a microprocessor where the luminance (ambient light level in lux) is derived using an empirical formula to approximate the human eye response.

Figure 21:
Detailed Block Diagram of TMD2772/TMD2772WA



A fully integrated proximity detection solution is provided with an 850-nm IR LED, LED driver circuit, and proximity detection engine. An internal LED driver pin (LDR) is externally connected to the LED cathode (LEDK) to provide a controlled LED sink current. This is accomplished with a proprietary current calibration technique that accounts for all variances in silicon, optics, package, and most important, IR LED output power. This eliminates or greatly reduces the need for factory calibration that is required for most discrete proximity sensor solutions. The device is factory calibrated to achieve a proximity count

reading at a specified distance with a specific number of pulses. In use, the number of proximity LED pulses can be programmed from 1 to 255 pulses, which allows different proximity distances to be achieved. Each pulse has a 16 µs period with a 7.2 µs on time.

Communication with the device is accomplished through a fast (up to 400 kHz), two-wire I^2C serial bus for easy connection to a microcontroller or embedded controller. The digital output of the device is inherently more immune to noise when compared to an analog photodiode interface.

The device provides a separate pin for level-style interrupts. When interrupts are enabled and a pre-set value is exceeded, the interrupt pin is asserted and remains asserted until cleared by the controlling firmware. The interrupt feature simplifies and improves system efficiency by eliminating the need to poll a sensor for a light intensity or proximity value. An interrupt is generated when the value of an ALS or proximity conversion exceeds either an upper or lower threshold. In addition, a programmable interrupt persistence feature allows the user to determine how many consecutive exceeded thresholds are necessary to trigger an interrupt. Interrupt thresholds and persistence settings are configured independently for both ALS and proximity.

Principles of Operation

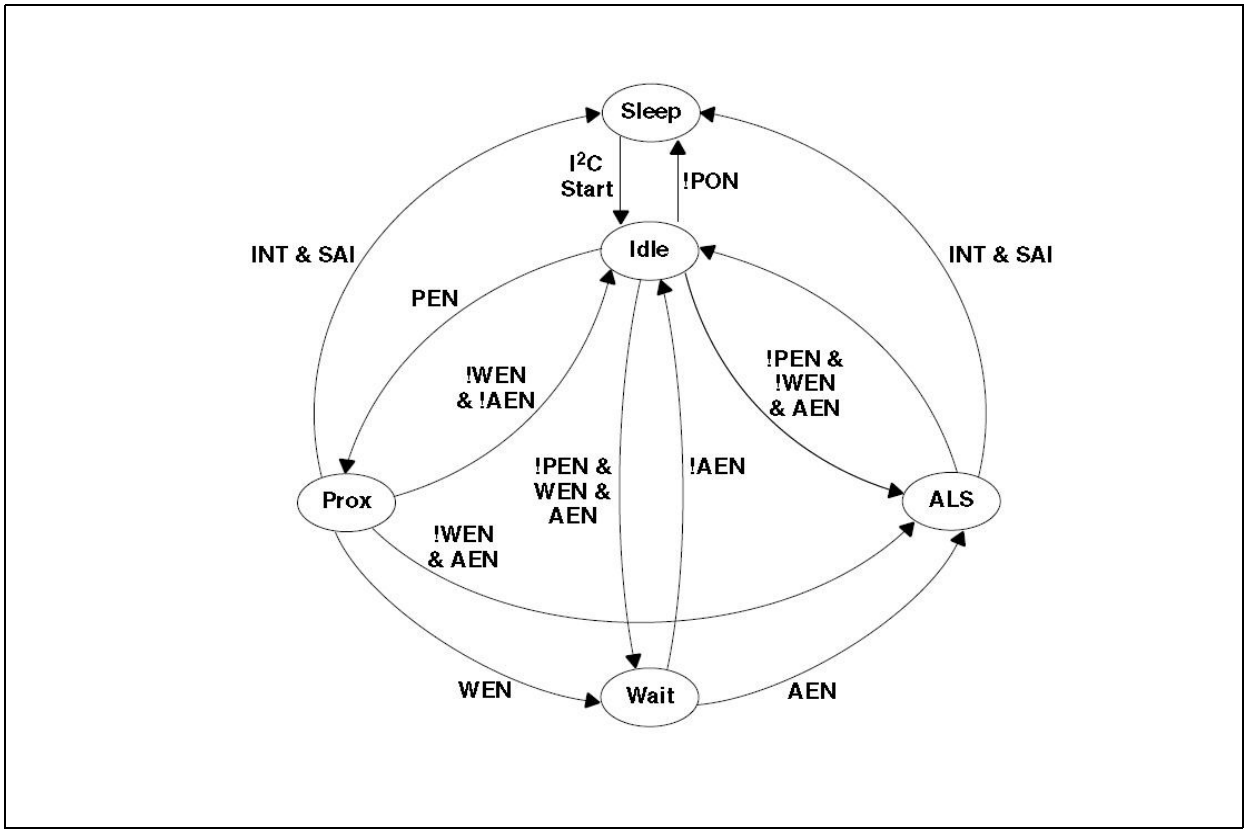
System State Machine

An internal state machine provides system control of the ALS, proximity detection, and power management features of the device. At power up, an internal power-on-reset initializes the device and puts it in a low-power Sleep state.

When a start condition is detected on the I^2C bus, the device transitions to the Idle state where it checks the Enable register (0x00) PON bit. If PON is disabled, the device will return to the Sleep state to save power. Otherwise, the device will remain in the Idle state until a proximity or ALS function is enabled. Once enabled, the device will execute the Prox, Wait, and ALS states in sequence as indicated in Figure 22. Upon completion and return to Idle, the device will automatically begin a new prox–wait–ALS cycle as long as PON and either PEN or AEN remain enabled.

If the Prox or ALS function generates an interrupt and the Sleep-After-Interrupt (SAI) feature is enabled, the device will transition to the Sleep state and remain in a low-power mode until an I^2C command is received. See Interrupts for additional information.

Figure 22:
Simplified State Diagram



Photodiodes

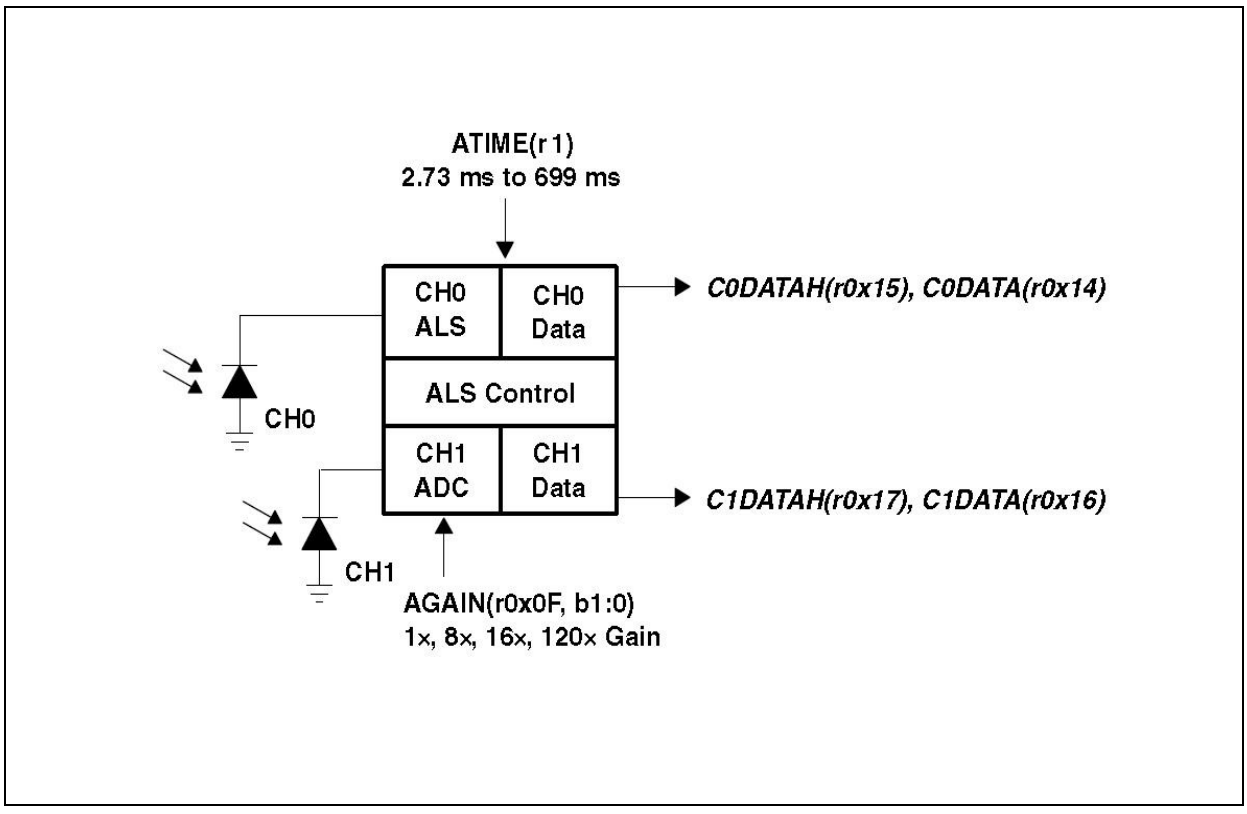
Conventional ALS detectors respond strongly to infrared light, which the human eye does not see. This can lead to significant error when the infrared content of the ambient light is high (such as with incandescent lighting).

This problem is overcome through the use of two photodiodes. The Channel 0 photodiode, referred to as the CH0 channel, is sensitive to both visible and infrared light, while the Channel 1 photodiode, referred to as CH1, is sensitive primarily to infrared light. Two integrating ADCs convert the photodiode currents to digital outputs. The ADC digital outputs from the two channels are used in a formula to obtain a value that approximates the human eye response in units of lux.

ALS Operation

The ALS engine contains ALS gain control (AGAIN) and two integrating analog-to-digital converters (ADC), one for the CH0 and one for the CH1 photodiodes. The ALS integration time (ATIME) impacts both the resolution and the sensitivity of the ALS reading. Integration of both channels occurs simultaneously and upon completion of the conversion cycle, the results are transferred to the data registers (C0DATA and C1DATA). This data is also referred to as channel count. The transfers are double-buffered to ensure data integrity.

Figure 23:
ALS Operation



The registers for programming the integration and wait times are a 2's compliment values. The actual time can be calculated as follows:

ATIME = 256 – Integration Time / 2.73 ms

Inversely, the time can be calculated from the register value as follows:

Integration Time = 2.73 ms × (256 – ATIME)

In order to reject 50/60 Hz ripple strongly present in fluorescent lighting, the integration time needs to be programmed in multiples of 10 / 8.3 ms or the half cycle time. Both frequencies can be rejected with a programmed value of 50 ms (ATIME = 0xED) or multiples of 50 ms (i.e. 100, 150, 200, 400, 600).

The registers for programming the AGAIN hold a two-bit value representing a gain of 1×, 8×, 16×, or 120×. The gain, in terms of amount of gain, will be represented by the value AGAINx, i.e. AGAINx = 1, 8, 16, or 120. With the AGL bit set, the gains will be lowered to 1/6, 8/6, 16/6, and 20×, allowing for up to 60k lux.

Lux Equation

The lux calculation is a function of CH0 channel count (C0DATA), CH1 channel count (C1DATA), ALS gain (AGAINx), and ALS integration time in milliseconds (ATIME_ms). If an aperture, glass/plastic, or a light pipe attenuates the light equally across the spectrum (300 nm to 1100 nm), then a scaling factor referred to as glass attenuation (GA) can be used to compensate for attenuation. For a device in open air with no aperture or glass/plastic above the device, GA = 1. If it is not spectrally flat, then a custom lux equation with new coefficients should be generated. (See **ams** application note).

Counts per Lux (CPL) needs to be calculated only when ATIME or AGAIN is changed, otherwise it remains a constant. The first segment of the equation (Lux1) covers fluorescent and incandescent light. The second segment (Lux2) covers dimmed incandescent light. The final lux is the maximum of Lux1, Lux2, or 0.

Lux formula for **TMD2772**:

CPL = (ATIME_ms × AGAINx) / 20

Lux1 = (C0DATA – (1.75 × C1DATA)) / CPL

Lux2 = ((0.63 × C0DATA) – (1.00 × C1DATA)) / CPL

Lux = MAX(Lux1, Lux2, 0)

Lux formula for **TMD2772WA**:

CPL = (ATIME_ms × AGAINx) / 1.16

Lux1 = (C0DATA - (1.8422 x C1DATA)) / CPL

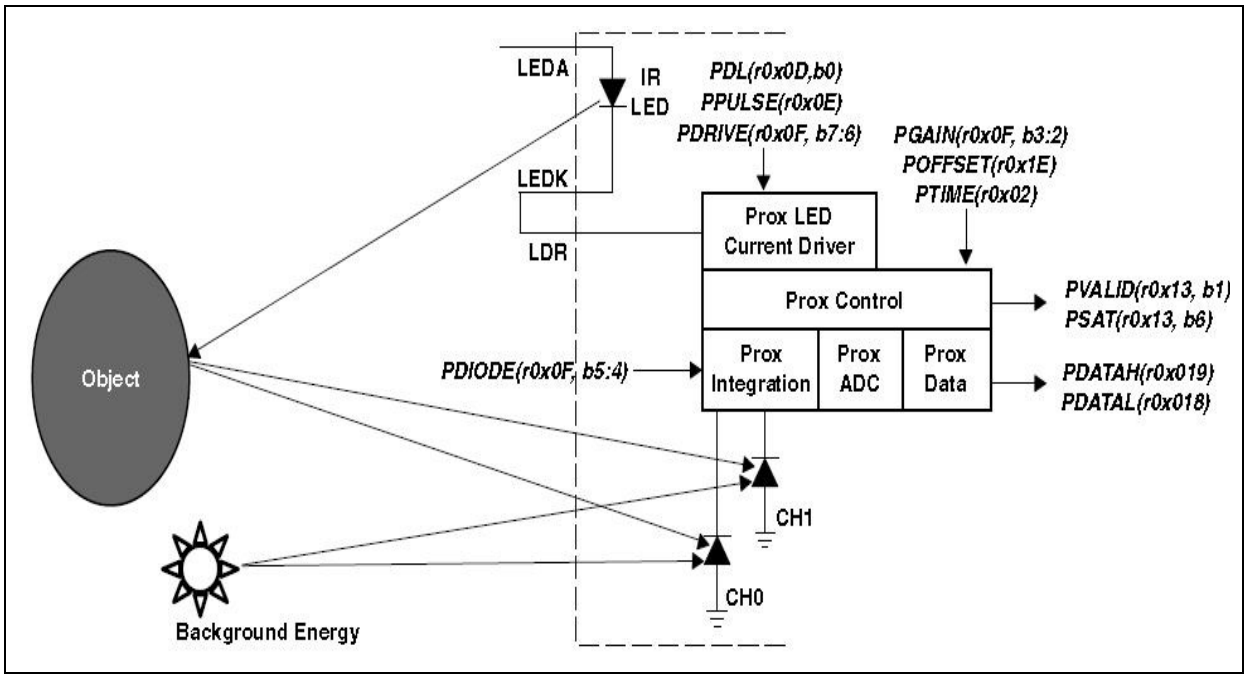
Lux2 = ((0.4106 x C0DATA) - (0.667 x C1DATA)) / CPL

Lux = MAX(Lux1, Lux2, 0)

Proximity Detection

Proximity detection is accomplished by measuring the amount of I_R energy, from the internal IR LED, reflected off an object to determine its distance. The internal proximity IR LED is driven by the integrated proximity LED current driver as shown in Figure 24.The proximity detector will see light reflected from the intended target as well as light reflected through any path. Both surfaces of a transparent cover will reflect some of the IR LEDs energy. An air gap of less the 0.5mm between the top of the module and the cover is recommended. For a detailed explanation of the of the effects of an air gap see **ams** application note; Application Note DN58: *Proximity Detection Behind Glass* for a detailed discussion of optical design considerations.

Figure 24:
Proximity Detection



The LED current driver, output on the LDR terminal, provides a regulated current sink that eliminates the need for an external current limiting resistor. The combination of proximity LED drive strength (PDRIVE) and proximity drive level (PDL) determine the drive current. PDRIVE sets the drive current to 100%, 50%, 25%, or 12.5% when PDL is not asserted. However, when PDL is asserted, the drive current is reduced by a factor of 9.

Referring to the Detailed State Machine figure, the LED current driver pulses the IR LED as shown in Figure 25 during the Prox Accum state. Figure 25 also illustrates that the LED On pulse has a fixed width of 7.3µs and period of 16.0µs. So, in addition to setting the proximity drive current, 1 to 255 proximity pulses (PPULSE) can be programmed. When deciding on the number

of proximity pulses, keep in mind that the signal increases proportionally to PPULSE, while noise increases by the square root of PPULSE.

Figure 25:
Proximity LED Current Driver Waveform

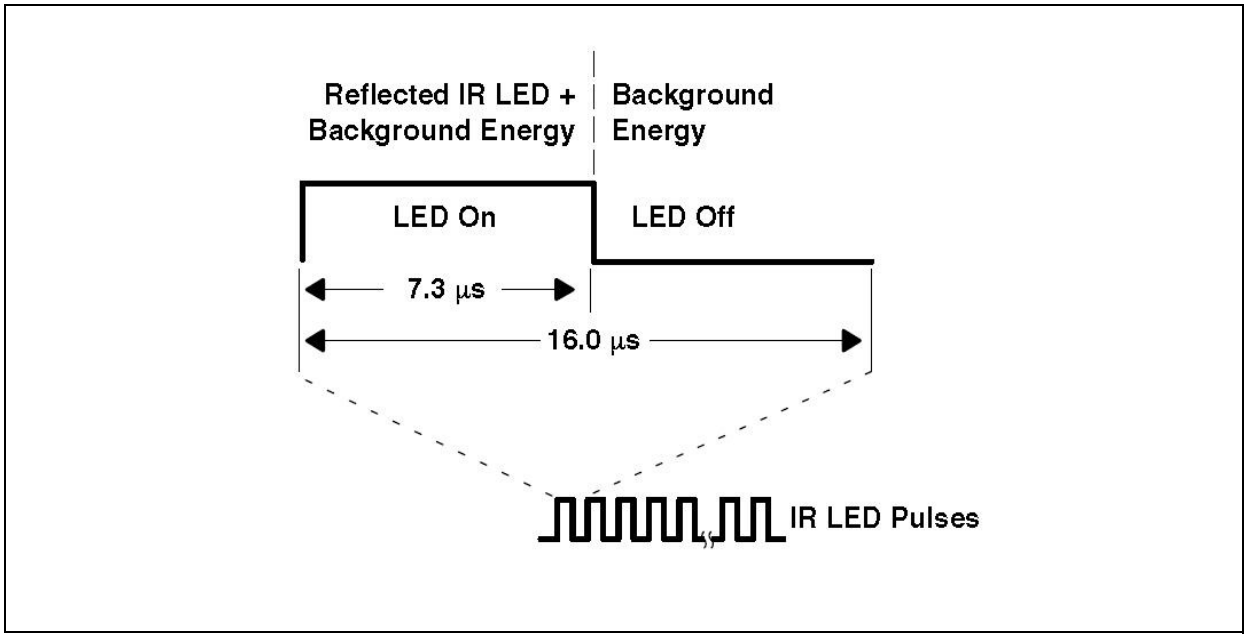


Figure 24 illustrates light rays emitting from the internal IR LED, reflecting off an object, and being absorbed by the CH0 and CH1 photodiodes. The proximity diode selector (PDIODE) determines which of the two photodiodes is used for a given proximity measurement. Note that neither photodiode is selected when the device first powers up, so PDIODE must be set for proximity detection to work.

Referring again to Figure 25, the reflected IR LED and the background energy is integrated during the LED On time, then during the LED Off time, the integrated background energy is subtracted from the LED On time energy, leaving the IR LED energy to accumulate from pulse to pulse. The proximity gain (PGAIN) determines the integration rate, which can be programmed to 1×, 2×, 4×, or 8× gain. At power up, PGAIN defaults to 1× gain, which is recommended for most applications. For reference, PGAIN equal to 4× is comparable to the TMD2771's 1× gain setting. During LED On time integration, the proximity saturation bit in the Status register (0x13) will be set if the integrator saturates. This condition can occur if the proximity gain is set too high for the lighting conditions, such as in the presence of bright sunlight. Once asserted, PSAT will remain set until a special function proximity interrupt clear command is received from the host. See Command Register

After the programmed number of proximity pulses have been generated, the proximity ADC converts and scales the proximity measurement to a 16-bit value, then stores the result in two 8-bit proximity data (PDATAx) registers. ADC scaling is controlled by the proximity ADC conversion time (PTIME) which

is programmable from 1 to 256 2.73ms time units. However, depending on the application, scaling the proximity data will equally scale any accumulated noise. Therefore, in general, it is recommended to leave PTIME at the default value of one 2.73ms ADC conversion time (0xFF).

In many practical proximity applications, a number of optical system and environmental conditions can produce an offset in the proximity measurement result. To counter these effects, a proximity offset (POFFSET) is provided which allows the proximity data to be shifted positive or negative. Additional information on the use of the proximity offset feature is provided in available **ams** application notes.

Once the first proximity cycle has completed, the proximity valid (PVALID) bit in the Status register will be set and remain set until the proximity detection function is disabled (PEN).

For additional information on using the proximity detection function behind glass and for optical system design guidance, please see available **ams** application notes.

Interrupts

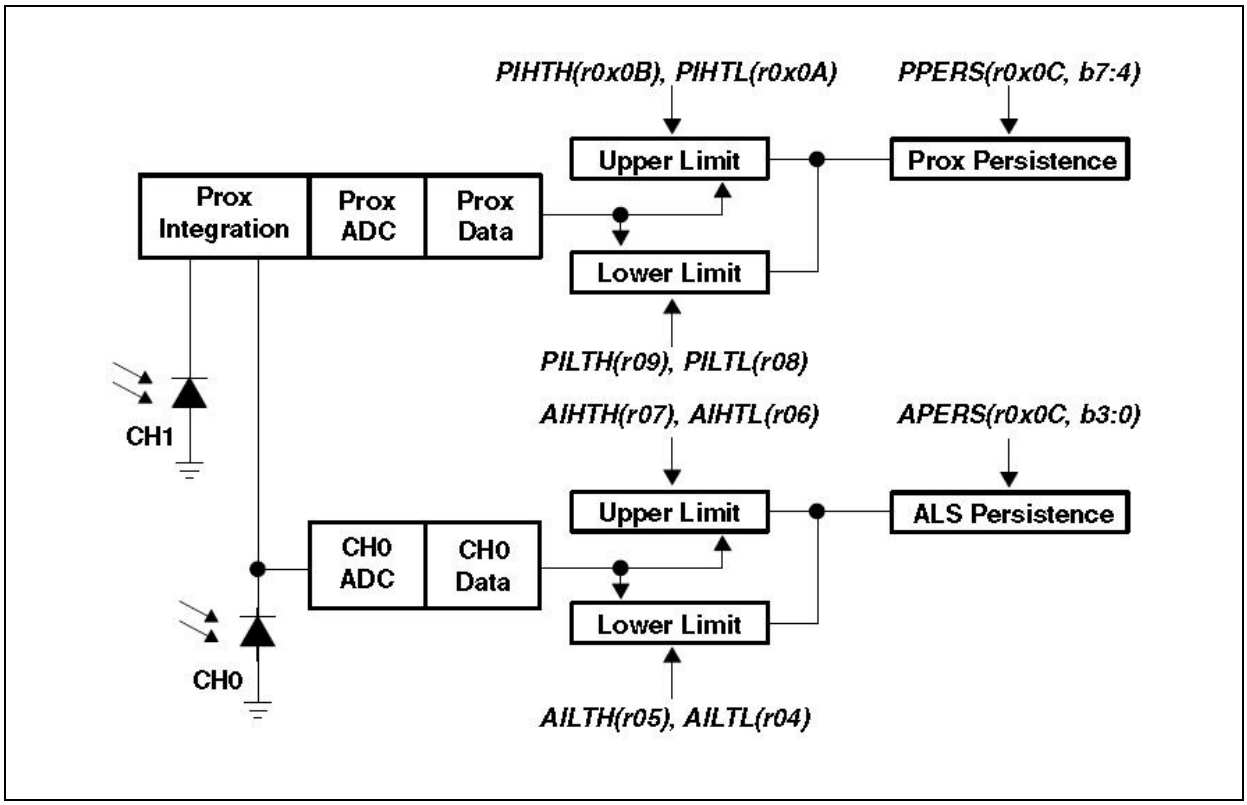
The interrupt feature simplifies and improves system efficiency by eliminating the need to poll the sensor for light intensity or proximity values outside of a user-defined range. While the interrupt function is always enabled and its status is available in the status register (0x13), the output of the interrupt state can be enabled using the proximity interrupt enable (PIEN) or ALS interrupt enable (AIEN) fields in the enable register (0x00).

Four 16-bit interrupt threshold registers allow the user to set limits below and above a desired light level and proximity range. An interrupt can be generated when the ALS CH0 data (C0DATA) falls outside of the desired light level range, as determined by the values in the ALS interrupt low threshold registers (AILTx) and ALS interrupt high threshold registers (AIHTx). Likewise, an out-of-range proximity interrupt can be generated when the proximity data (PDATA) falls below the proximity interrupt low threshold (PILTx) or exceeds the proximity interrupt high threshold (PIHTx).

It is important to note that the thresholds are evaluated in sequence, first the low threshold, then the high threshold. As a result, if the low threshold is set above the high threshold, the high threshold is ignored and only the low threshold is evaluated.

To further control when an interrupt occurs, the device provides a persistence filter. The persistence filter allows the user to specify the number of consecutive out-of-range ALS or proximity occurrences before an interrupt is generated. The Interrupt register (0x0C) allows the user to set the ALS persistence filter (APERS) and the proximity persistence filter (PPERS) values. See the Interrupt Register (0x0C) for details on the persistence filter values. Once the persistence filter generates an interrupt, it will continue until a special function interrupt clear command is received. See Command Register

Figure 26:
Programmable Interrupt



System State Machine Timing

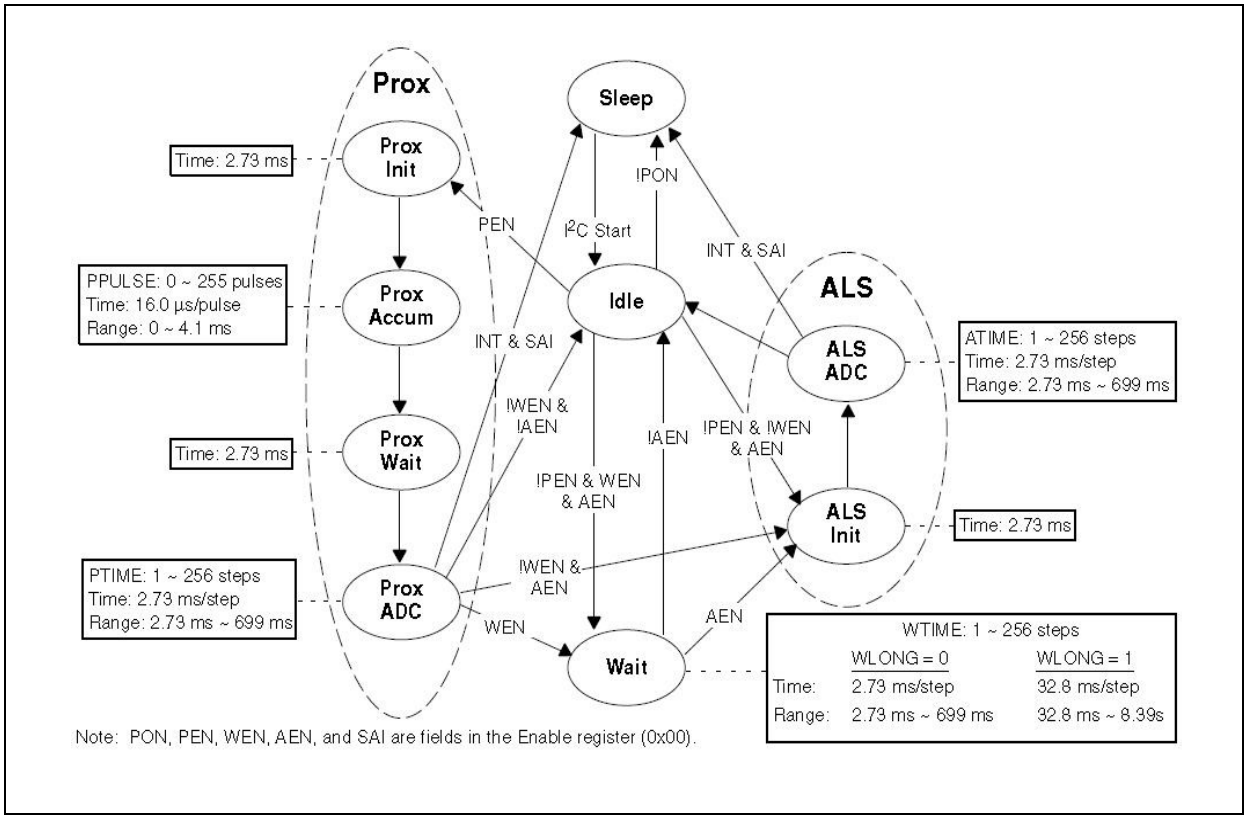
The system state machine shown in Figure 27 provides an overview of the states and state transitions that provide system control of the device. This section highlights the programmable features, which affect the state machine cycle time, and provides details to determine system level timing.

When the proximity detection feature is enabled (PEN), the state machine transitions through the Prox Init, Prox Accum, Prox Wait, and Prox ADC states. The Prox Init and Prox Wait times are a fixed 2.73 ms, whereas the Prox Accum time is determined by the number of proximity LED pulses (PPULSE) and the Prox ADC time is determined by the integration time (PTIME). The formulas to determine the Prox Accum and Prox ADC times are given in the associated boxes in Figure 27. If an interrupt is generated as a result of the proximity cycle, it will be asserted at the end of the Prox ADC state and transition to the Sleep state if SAI is enabled.

When the power management feature is enabled (WEN), the state machine will transition in turn to the Wait state. The wait time is determined by WLONG, which extends normal operation by 12× when asserted, and WTIME. The formula to determine the wait time is given in the box associated with the Wait state in Figure 27.

When the ALS feature is enabled (AEN), the state machine will transition through the ALS Init and ALS ADC states. The ALS Init state takes 2.73 ms, while the ALS ADC time is dependent on the integration time (ATIME). The formula to determine ALS ADC time is given in the associated box in Figure 27. If an interrupt is generated as a result of the ALS cycle, it will be asserted at the end of the ALS ADC state and transition to the Sleep state if SAI is enabled.

Figure 27:
Detailed State Machine



Power Management

Power consumption can be managed with the Wait state, because the Wait state typically consumes only 90µA of I_{DD} current. An example of the power management feature is given below. With the assumptions provided in the example, average I_{DD} is estimated to be 176µA.

Figure 28:
Power Management

System State Machine State	Programmable Parameter	Programmed Value	Duration	Typical Current
Prox Init			2.73 ms	0.195 mA
Prox Accum	PPULSE	0x04	0.064 ms	
Prox Accum – LED On			0.029 ms (1)	103 mA
Prox Accum – LED OFF			0.035 ms (2)	0.195 mA
Prox Wait			2.73 ms	0.195 mA
Prox ADC	PTIME	0xFF	2.73 ms	0.195 mA
Wait	WTIME	0xEE	49 2 ms	0 090 mA
	WLONG			
ALS Init			2.73 ms	0.195 mA
ALS ADC	ATIME	0xEE	49 2 ms	0.195 mA

Note(s):

1. Prox Accum – LED On time = 7.3 µs per pulse × 4 pulses = 29.3µs = 0.029 ms
2. Prox Accum – LED Off time = 8.7 µs per pulse × 4 pulses = 34.7µs = 0.035 ms

Average I_{DD} Current =
((0.029 × 103) + (0.035 x 0.195) + (2.73 × 0.195) + (49.2 × 0.090) + (49.2 × 0.195) + (2.73 × 0.195 × 3)) / 109 ≈ 176 µA.

Keeping with the same programmed values as the example, Figure 29 shows how the average I_{DD} current is affected by the Wait state time, which is determined by WEN, WTIME, and WLONG. Note that the worst-case current occurs when the Wait state is not enabled.

Figure 29:
Average I_{DD} Current

WEN	WTIME	WLONG	WAIT State	Average I_{DD} Current
0	n/a	n/a	0 ms	245 µA
1	0xFF	0	2.73 ms	238 µA
1	0xEE	0	49.2 ms	175 µA
1	0x00	0	699 ms	102 µA
1	0x00	1	8389 ms	91 µA

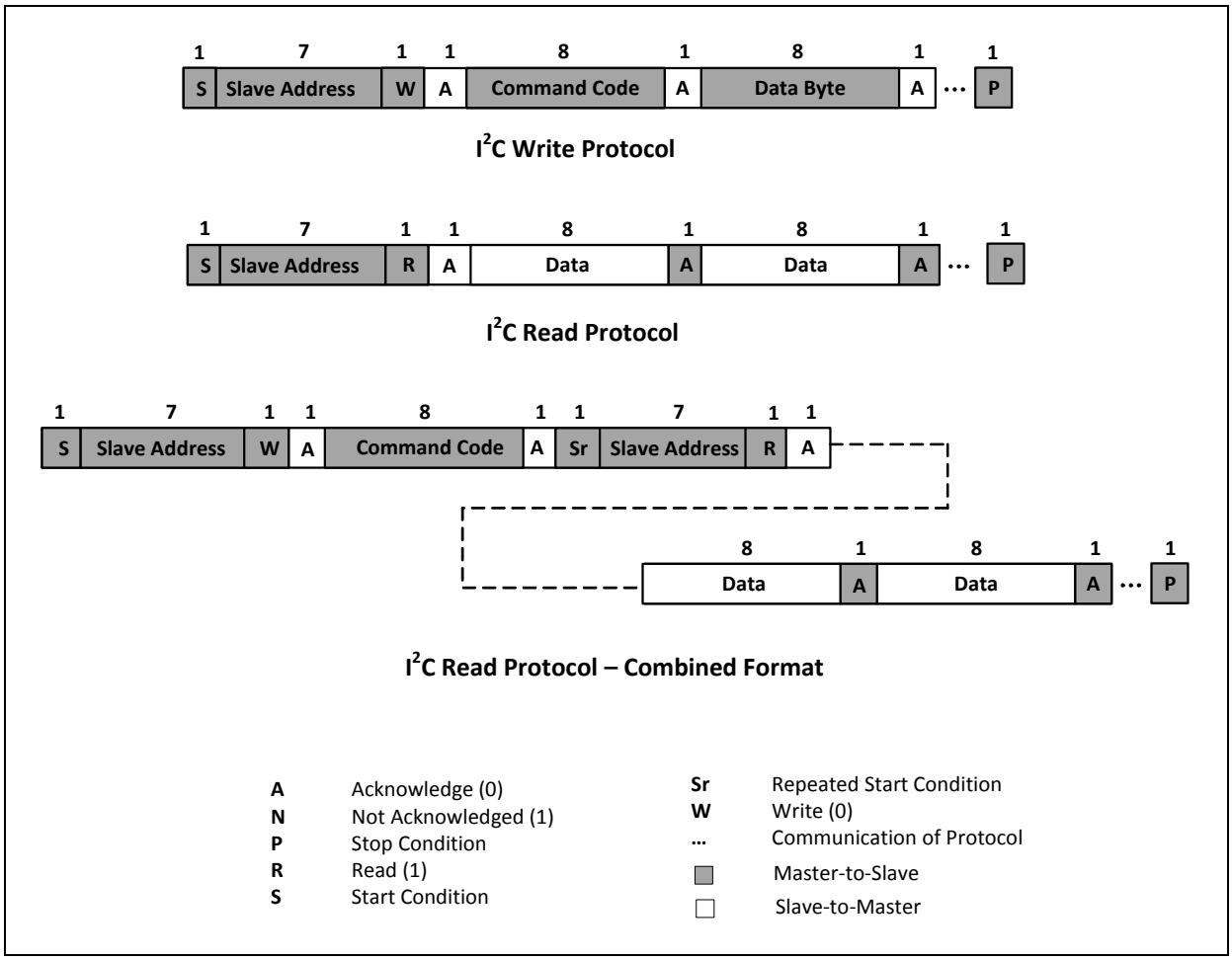
I²C Protocol

Interface and control are accomplished through an I²C serial compatible interface (standard or fast mode) to a set of registers that provide access to device control functions and output data. The devices support the 7-bit I²C addressing protocol.

The I²C standard provides for three types of bus transaction: read, write, and a combined protocol (Figure 30). During a write operation, the first byte written is a command byte followed by data. In a combined protocol, the first byte written is the command byte followed by reading a series of bytes. If a read command is issued, the register address from the previous command will be used for data access. Likewise, if the MSB of the command is not set, the device will write a series of bytes at the address stored in the last valid command with a register address. The command byte contains either control information or a 5-bit register address. The control commands can also be used to clear interrupts.

The I²C bus protocol was developed by Phillips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification at
http://www.i2c-bus.org/references/

Figure 30:
I²C Protocols



Register Description

The device is controlled and monitored by data registers and a command register accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions. The register set is summarized in Figure 31.

Figure 31:
Register Map

Address	Register Name	R/W	Register Function	Reset Value
---	COMMAND	W	Specifies register address	0x00
0x00	ENABLE	R/W	Enables states and interrupts	0x00
0x01	ATIME	R/W	Integration time	0xFF
0x02	PTIME	R/W	Proximity ADC time	0xFF
0x03	WTIME	R/W	Wait time	0xFF
0x04	AILTL	R/W	ALS interrupt low threshold low byte	0x00
0x05	AILTH	R/W	ALS interrupt low threshold high byte	0x00
0x06	AIHTL	R/W	ALS interrupt high threshold low byte	0x00
0x07	AIHTH	R/W	ALS interrupt high threshold high byte	0x00
0x08	PILTL	R/W	Proximity interrupt low threshold low byte	0x00
0x09	PILTH	R/W	Proximity interrupt low threshold high byte	0x00
0x0A	PIHTL	R/W	Proximity interrupt high threshold low byte	0x00
0x0B	PIHTH	R/W	Proximity interrupt high threshold high byte	0x00
0x0C	PERS	R/W	Interrupt persistence filters	0x00
0x0D	CONFIG	R/W	Configuration	0x00
0x0E	PPULSE	R/W	Proximity pulse count	0x00
0x0F	CONTROL	R/W	Control register	0x00
0x11	REVISION	R	Die revision number	Rev Num
0x12	ID	R	Device ID	0x39

Address	Register Name	R/W	Register Function	Reset Value
0x13	STATUS	R	Device status	0x00
0x14	C0DATA	R	Ch0 ADC low data register	0x00
0x15	C0DATAH	R	Ch0 ADC high data register	0x00
0x16	C1DATA	R	Ch1 ADC low data register	0x00
0x17	C1DATAH	R	Ch1 ADC high data register	0x00
0x18	PDATAL	R	Proximity ADC low data register	0x00
0x19	PDATAH	R	Proximity ADC high data register	0x00
0x1E	POFFSET	R/W	Proximity offset register	0x00

The mechanics of accessing a specific register depends on the specific protocol used (see I²C Protocol). In general, the COMMAND register is written first to specify the specific control/status register for following read/write operations.

Command Register

The Command Register specifies the address of the target register for future write and read operations. The command register defaults to 0x00 at power-on.

Figure 32:
Command Register

7	6	5	4	3	2	1	0
COMMAND	TYPE		ADD				

Field	Bits	Description (Reset value = 0x00)	
COMMAND	7	**Select Command Register**. Must write as 1 when addressing COMMAND register.	
TYPE	6:5	Selects type of transaction to follow in subsequent data transfers:	
		Field Value	**Description**
		00	Repeated byte protocol transaction
		01	Auto-increment protocol transaction
		10	Reserved — Do not use
		11	Special function – See description below
		Transaction type 00 will repeatedly read the same register with each data access. Transaction type 01 will provide an auto-increment function to read successive register bytes.	
ADD	4:0	**Address field/special function field.** Depending on the transaction type, see above, this field either specifies a special function command or selects the specific control-status-register for following write and read transactions. The field values listed below apply only to special function commands:	
		Field Value	**Description**
		00000	Normal — no action
		00101	Proximity interrupt clear
		00110	ALS interrupt clear
		00111	Proximity and ALS interrupt clear
		other	Reserved — Do not write
		ALS/Proximity Interrupt Clear clears any pending ALS/Proximity interrupt. This special function is self clearing.	

Enable Register (0x00)

The Enable Register is used to power the device on/off, enable functions, and interrupts.

Figure 33:
Enable Register

7	6	5	4	3	2	1	0
Reserved	SAI	PIEN	AIEN	WEN	PEN	AEN	PON

Field	Bits	Description (Reset value = 0x00)
Reserved	7	**Reserved.** Write as 0.
SAI	6	**Sleep after interrupt.** When asserted, the device will power down at the end of a proximity or ALS cycle if an interrupt has been generated.
PIEN	5	**Proximity interrupt mask.** When asserted, permits proximity interrupts to be generated.
AIEN	4	**ALS interrupt mask**. When asserted, permits ALS interrupt to be generated.
WEN	3	**Wait Enable.** This bit activates the wait feature. Writing a 1 activates the wait timer. Writing a 0 disables the wait timer.
PEN	2	**Proximity Enable**. This bit activates the proximity function. Writing a 1 enables proximity. Writing a 0 disables proximity.
AEN	1	**ALS Enable.** This bit activates the two channel ADC. Writing a 1 activates the ALS. Writing a 0 disables the ALS.
PON	0	**Power ON.** This bit activates the internal oscillator to permit the timers and ADC channels to operate. Writing a 1 activates the oscillator. Writing a 0 disables the oscillator.

ALS Time Register (0x01)

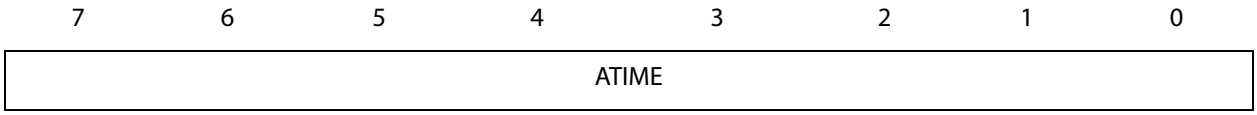
The ALS Time Register controls the internal integration time of the ALS channel ADS's in 2.73ms increments. Time is expressed as a 2's complement number.

To calculate the value:

1. Determine the number of 2.73ms intervals required
2. Take the 2's complement

For a 1 x 2.73ms interval, 0xFF should be written. For 2 x 2.73ms intervals, 0xFE should be written. The maximum integration time is 699ms (0x00).

Figure 34:
ALS Time Register



Field	Bits	Description (Reset value = 0xFF)			
		Value	Cycles	Time	Max Count
ATIME	7:0	0xFF	1	2.73 ms	1024
		0xF6	10	27.3 ms	10240
		0xDB	37	101 ms	37888
		0xC0	64	175 ms	65535
		0x00	256	699 ms	65535

Proximity Time Register (0x02)

The Proximity Time Register controls the integration time of the proximity ADC in 2.73 ms increments. Time is expressed as a 2's complement number. It is recommended that this register be programmed to a value of 0xFF (1 integration cycle).

Figure 35:
Proximity Time Register

7	6	5	4	3	2	1	0
PTIME							

Field	Bits	Description (Reset value = 0xFF)			
		Value	Cycles	Time	Max Count
PTIME	7:0	0xFF	1	2.73 ms	1023

Wait Time Register (0x03)

Wait time is set in 2.73 ms increments unless the WLONG bit is asserted in which case the wait times are 12x longer. WTIME is programmed as a 2's complement number.

Figure 36:
Wait Time Register

7	6	5	4	3	2	1	0
WTIME							

Field	Bits	Description (Reset value = 0xFF)			
		Register Value	Wait Time	Time (WLONG=0)	Time (WLONG=1)
WTIME	7:0	0xFF	1	2.73 ms	0.033 s
		0xB6	74	202 ms	2.4 s
		0x00	256	699 ms	8.4 s

Note(s):

1. The Proximity Wait Time Register should be configured before PEN and/or AEN is/are asserted.

ALS Interrupt Threshold Register (0x04 – 0x07)

The ALS Interrupt Threshold Registers provide the values to be used as the high and low trigger points for the comparison function for interrupt generation. If C0DATA is not between the low and high thresholds and the persistence criteria is met, an interrupt is asserted on the interrupt pin.

Figure 37:
ALS Interrupt Threshold Registers

Register	Address	Bits	Description (Reset value = 0x00)
AILTL	0x04	7:0	ALS low threshold lower byte
AILTH	0x05	7:0	ALS low threshold upper byte
AIHTL	0x06	7:0	ALS high threshold lower byte
AIHTH	0x07	7:0	ALS high threshold upper byte

Proximity Interrupt Threshold Register (0x08 – 0x0B)

The Proximity Interrupt Threshold Registers provide the values to be used as the high and low trigger points for the comparison function for interrupt generation. If the value generated by proximity channel is not between the low and high thresholds and the persistence criteria is met, an interrupt is signaled to the host processor.

Figure 38:
Proximity Interrupt Threshold Registers

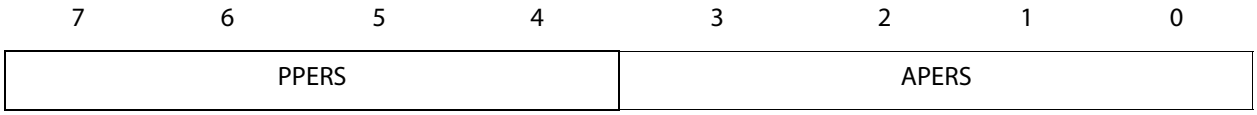
Register	Address	Bits	Description (Reset value = 0x00)
PILTL	0x08	7:0	Proximity low threshold lower byte
PILTH	0x09	7:0	Proximity low threshold upper byte
PIHTL	0x0A	7:0	Proximity high threshold lower byte
PIHTH	0x0B	7:0	Proximity high threshold upper byte

Interrupt Register (0x0C)

The Interrupt Register controls the filtering interrupt capabilities of the device. Configurable filtering is provided to allow interrupts to be generated after each ADC integration cycle or if the ADC integration has produced a result that is outside of the values specified by threshold register for some specified amount of time. Separate filtering is provided for proximity and ALS functions.

ALS interrupts are generated by looking only at the C0DATA ADC integration results.

Figure 39:
Interrupt Register



Field	Bits	Description (Reset value = 0x00)		
PPERS	7:4	**Proximity interrupt persistence filter.** Controls rate of proximity interrupt to the host processor.		
		Field Value	**Meaning**	**Interrupt Persistence**
		0000	Every	Every proximity cycle generates an interrupt
		0001	1	1 proximity value outside of threshold range
		0010	2	2 consecutive proximity values out of range
		…	…	…
		1111	15	15 consecutive proximity values out of range

Field	Bits	Description (Reset value = 0x00)		
APERS	3:0	**ALS Interrupt persistence filter.** Controls rate of interrupt to the host processor.		
		Field Value	**Persistence**	**Interrupt Persistence**
		0000	Every	Every ALS cycle generates an interrupt
		0001	1	1 value outside of threshold range
		0010	2	2 consecutive values out of range
		0011	3	3 consecutive values out of range
		0100	5	5 consecutive values out of range
		0101	10	10 consecutive values out of range
		0110	15	15 consecutive values out of range
		0111	20	20 consecutive values out of range
		1000	25	25 consecutive values out of range
		1001	30	30 consecutive values out of range
		1010	35	35 consecutive values out of range
		1011	40	40 consecutive values out of range
		1100	45	45 consecutive values out of range
		1101	50	50 consecutive values out of range
		1110	55	55 consecutive values out of range
		1111	60	60 consecutive values out of range

Configuration Register (0x0D)

The Configuration Register sets the proximity LED drive level, wait long time, and ALS gain level

Figure 40:
Configuration Register.

7	6	5	4	3	2	1	0
Reserved					AGL	WLONG	PDL

Field	Bits	Description (Reset value = 0x00)
Reserved	7:3	**Reserved.** Write as 0.
AGL	2	**ALS Gain Level.** When asserted, the 1× and 8× ALS gain (AGAIN) modes are scaled by 0.16. Otherwise, AGAIN is scaled by 1. Should be set = 0 anytime AGAIN is greater than 8x, or if using a TMD module.
WLONG	1	**Wait Long.** When asserted, the wait cycles are increased by a factor 12x from that programmed in the WTIME register.
PDL	0	**Proximity drive level.** When asserted, the proximity LDR drive current is reduced by 9.

Proximity Pulse Count Register (0x0E)

The Proximity Pulse Count Register sets the number of proximity pulses that the LDR pin will generate during the Prox Accum state. The pulses are generated at a 62.5kHz rate.

Figure 41:
Proximity Pulse Count Register

7	6	5	4	3	2	1	0
PPULSE							

Field	Bits	Description
PPULSE	7:0	**Proximity Pulse Count.** Specifies the number of proximity pulses to be generated.

Control Register (0x0F)

The Control Register provides eight bits of miscellaneous control to the analog block. These bits typically control functions such as gain settings and/or diode selection.

Figure 42:
Control Register

7	6	5	4	3	2	1	0
PDRIVE		PDIODE		PGAIN		AGAIN	

Field	Bits	Description (Reset value = 0x00)		
PDRIVE [1]	7:6	**Proximity LED Drive Strength.**		
		Field Value	**LED Strength – PDL=0**	**LED Strength – PDL=1**
		00	100 %	11.1 %
		01	50 %	5.6 %
		10	25 %	2.8 %
		11	12.5 %	1.4 %
PDIODE	5:4	**Proximity Diode Selector.**		
		Field Value	**Diode Selection**	
		00	Proximity uses neither diode	
		01	Proximity uses the CH0 diode	
		10	Proximity uses the CH1 diode	
		11	Reserved — Do not write	
PGAIN	3:2	**Proximity Gain.**		
		Field Value	**Proximity Gain Value**	
		00	1x gain	
		01	2x gain	
		10	4x gain	
		11	8x gain	

Field	Bits	Description (Reset value = 0x00)	
AGAIN	1:0	**ALS Gain**	
		Field Value	**ALS Gain Value**
		00	1X Gain
		01	8X Gain
		10	16X Gain
		11	120X Gain

Note(s):

1. LED STRENGTH values are nominal operating values. Specifications can be found in the Proximity Characteristics table.

Revision Register (0x11)

The Revision Register shows the silicon revision number. It is a read-only register and shows the revision level of the silicon used internally.

Figure 43:
Revision Register

7	6	5	4	3	2	1	0
Reserved				DIE_REV			

Field	Bits	Description (Reset value = Rev Num)
RESERVED	7:4	**Reserved.**
DIE_REV	3:0	**Die revision number**

ID Register (0x12)

The ID Register provides the value for the part number. The ID register is a read-only register whose value never changes.

Figure 44:
ID Register

7	6	5	4	3	2	1	0
ID							

Field	Bit	Description (Reset value = ID)
ID	7:0	TMD27721 = 0x30
		TMD27723 = 0x39
		TMD27725 = 0x30
		TMD27727 = 0x39
		TMD27721WA = 0x30
		TMD27723WA = 0x39

Status Register (0x13)

The Status Register provides the internal status of the device. This register is read only.

Figure 45:
Status Register

7	6	5	4	3	2	1	0
Reserved	PSAT	PINT	AINT	Reserved		PVALID	AVALID

Field	Bits	Description (Reset value = 0x00)
Reserved	7	**Reserved.** Bit reads as 0.
PSAT	6	**Proximity Saturation.** Indicates the proximity measurement saturated.
PINT	5	**Proximity Interrupt.** Indicates that the device is asserting a proximity interrupt.
AINT	4	**ALS Interrupt.** Indicates that the device is asserting an ALS interrupt.
Reserved	3:2	**Reserved.** Bits read as 0.
PVALID	1	**Proximity Valid.** Indicates that the Proximity channel has completed an integration cycle after the PEN bit has been asserted.
AVALID	0	**ALS Valid.** Indicates that the ALS channels have completed an integration cycle after AEN has been asserted.

ADC Channel Data Registers (0x14 – 0x17)

ALS data is stored as two 16-bit values. To ensure the data is read correctly, a two-byte read I^2C transaction should be used with auto increment protocol bits set in the command register. With this operation, when the lower byte register is read, the upper eight bits are stored in a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if additional ADC integration cycles end between the reading of the lower and upper registers.

Figure 46:
ADC Channel Data Registers

Register	Address	Bits	Description (Reset value = 0x00)
C0DATA	0x14	7:0	ALS CH0 data low byte
C0DATAH	0x15	7:0	ALS CH0 data high byte
C1DATA	0x16	7:0	ALS CH1 data low byte
C1DATAH	0x17	7:0	ALS CH1 data high byte

Proximity Data Registers (0x18 – 0x19)

Proximity data is stored as a 16-bit value. To ensure the data is read correctly, a two-byte read I^2C transaction should be utilized with auto increment protocol bits set in the command register. With this operation, when the lower byte register is read, the upper eight bits are stored into a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if the next ADC cycle ends between the reading of the lower and upper registers.

Figure 47:
Proximity Data Registers

Register	Address	Bits	Description (Reset value = 0x00)
PDATAL	0x18	7:0	Proximity data low byte
PDATAH	0x19	7:0	Proximity data high byte

Proximity Offset Register (0x1E)

The 8-bit proximity offset register provides compensation for proximity offsets caused by device variations, optical crosstalk, and other environmental factors. Proximity offset is a sign-magnitude value where the sign bit, bit 7, determines if the offset is negative (bit 7 = 0) or positive (bit 7 = 1). The magnitude of the offset compensation depends on the proximity gain (PGAIN), proximity LED drive strength (PDRIVE), and the number of proximity pulses (PPULSE). Because a number of environmental factors contribute to proximity offset, this register is best suited for use in an adaptive closed-loop control system. See available **ams** application notes for proximity offset register application information.

The default value on power up is factory trimmed to provide a typical proximity offset of 100. This is achieved with no glass or reflective object above the sensor, and PPULSE=08, PGAIN=10, PDRIVE=00. If the value is changed during use but power is removed it will return to the default value on power up.

Figure 48:
Proximity Offset Register

7	6	5	4	3	2	1	0
SIGN	MAGNITUDE						

Field	Bits	Description (Reset value = trimmed value)
SIGN	7	**Proximity Offset Sign.** The offset sign shifts the proximity data negative when equal to 0 and positive when equal to 1.
MAGNITUDE	6:0	**Proximity Offset Magnitude.** The offset magnitude shifts the proximity data positive or negative, depending on the proximity offset sign. The actual amount of the shift depends on the proximity gain (PGAIN), proximity LED drive strength (PDRIVE), and the number of proximity pulses (PPULSE).

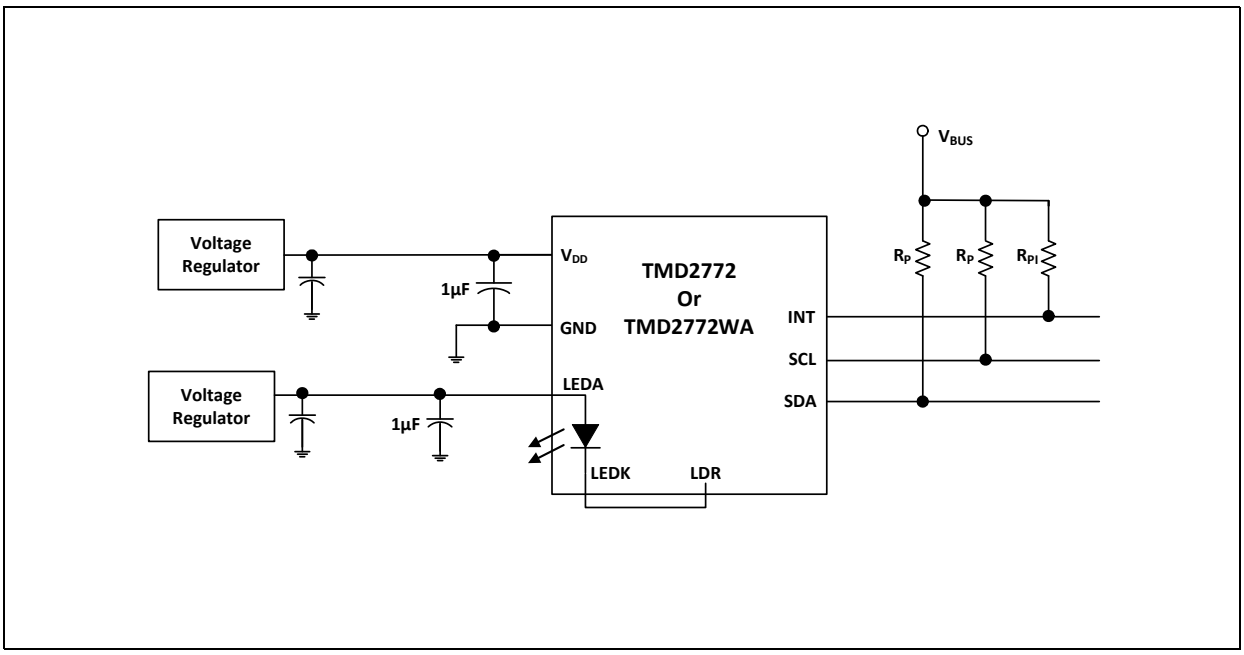
Application Information

LED Driver Pin with Proximity Detection

In a proximity sensing system, the included IR LED can be pulsed with more than 100 mA of rapidly switching current, therefore, a few design considerations must be kept in mind to get the best performance. The key goal is to reduce the power supply noise coupled back into the device during the LED pulses. Averaging of multiple proximity samples is recommended to reduce the proximity noise.

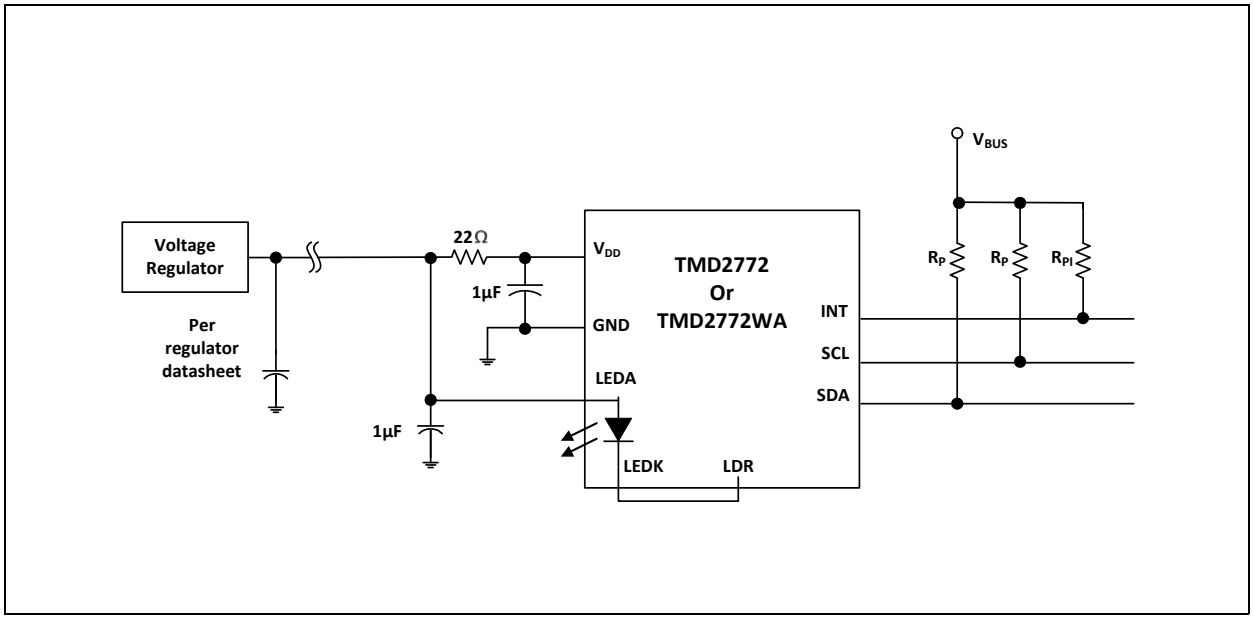
The first recommendation is to use two power supplies; one for the device V_{DD} and the other for the IR LED. In many systems, there is a quiet analog supply and a noisy digital supply. By connecting the quiet supply to the V_{DD} pin and the noisy supply to the LEDA pin, the key goal can be met. Place a 1µF low-ESR decoupling capacitor as close as possible to the V_{DD} pin and another at the LEDA pin, and at least 10µF of bulk capacitance to supply the 100mA current surge. This may be distributed as two 4.7µF capacitors.

Figure 49:
Proximity Sensing Using Separate Power Supplies



If it is not possible to provide two separate power supplies, the device can be operated from a single supply. A 22Ω resistor in series with the V_{DD} supply line and a 1µF low ESR capacitor effectively filter any power supply noise. The previous capacitor placement considerations apply.

Figure 50:
Proximity Sensing Using Single Power Supply



V_{BUS} in the above figures refers to the I^2C bus voltage which is either V_{DD} or 1.8V. Be sure to apply the specified I^2C bus voltage shown in the Available Options table for the specific device being used.

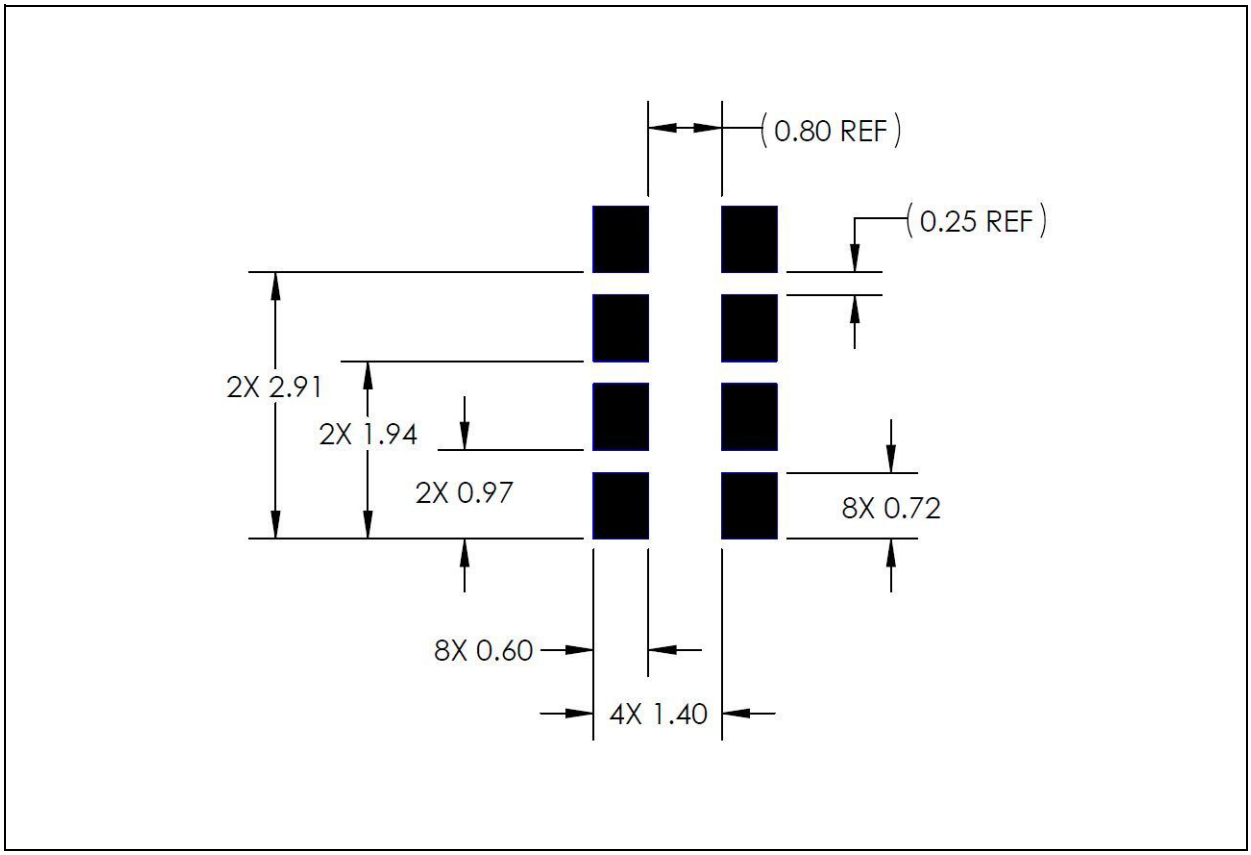
The I^2C signals and the Interrupt are open-drain outputs and require pull-up resistors. The pull-up resistor (RP) value is a function of the I^2C bus speed, the I^2C bus voltage, and the capacitive load. The **ams** EVM running at 400 kbps, uses 1.5kΩ resistors. A 10kΩ pull-up resistor (RPI) can be used for the interrupt line.

PCB Pad Layout

Suggested PCB pad layout guidelines for the surface mount module are shown below. Flash Gold is recommended surface finish for the landing pads.

This footprint is recommended for both the TMD2772 and the TMD2772WA.

Figure 51:
Suggested Module PCB Layout

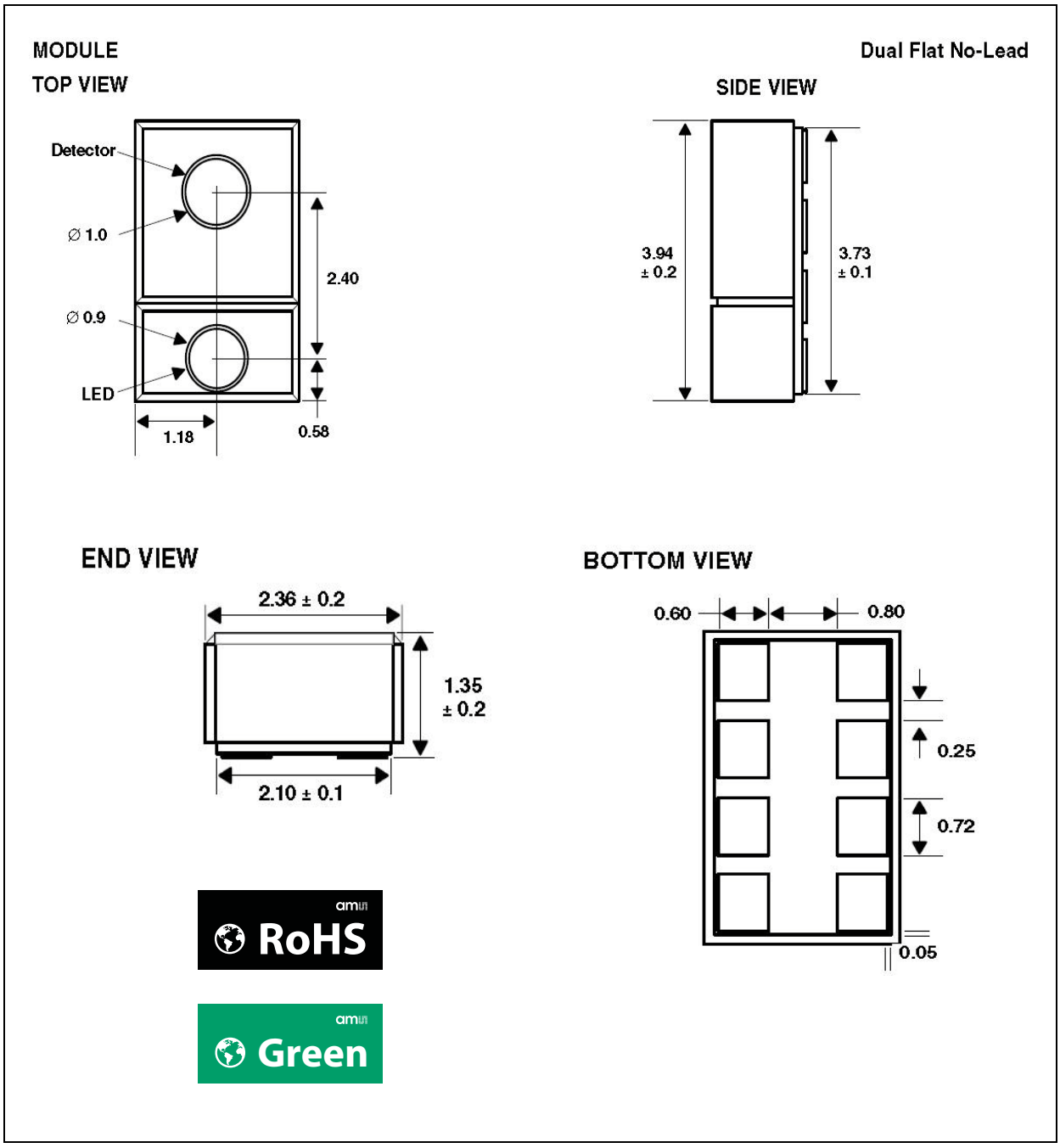


Note(s):

1. All linear dimensions are in millimeters.
2. Dimension tolerances are ±0.05mm unless otherwise noted.
3. This drawing is subject to change without notice.

Packaging Mechanical Data

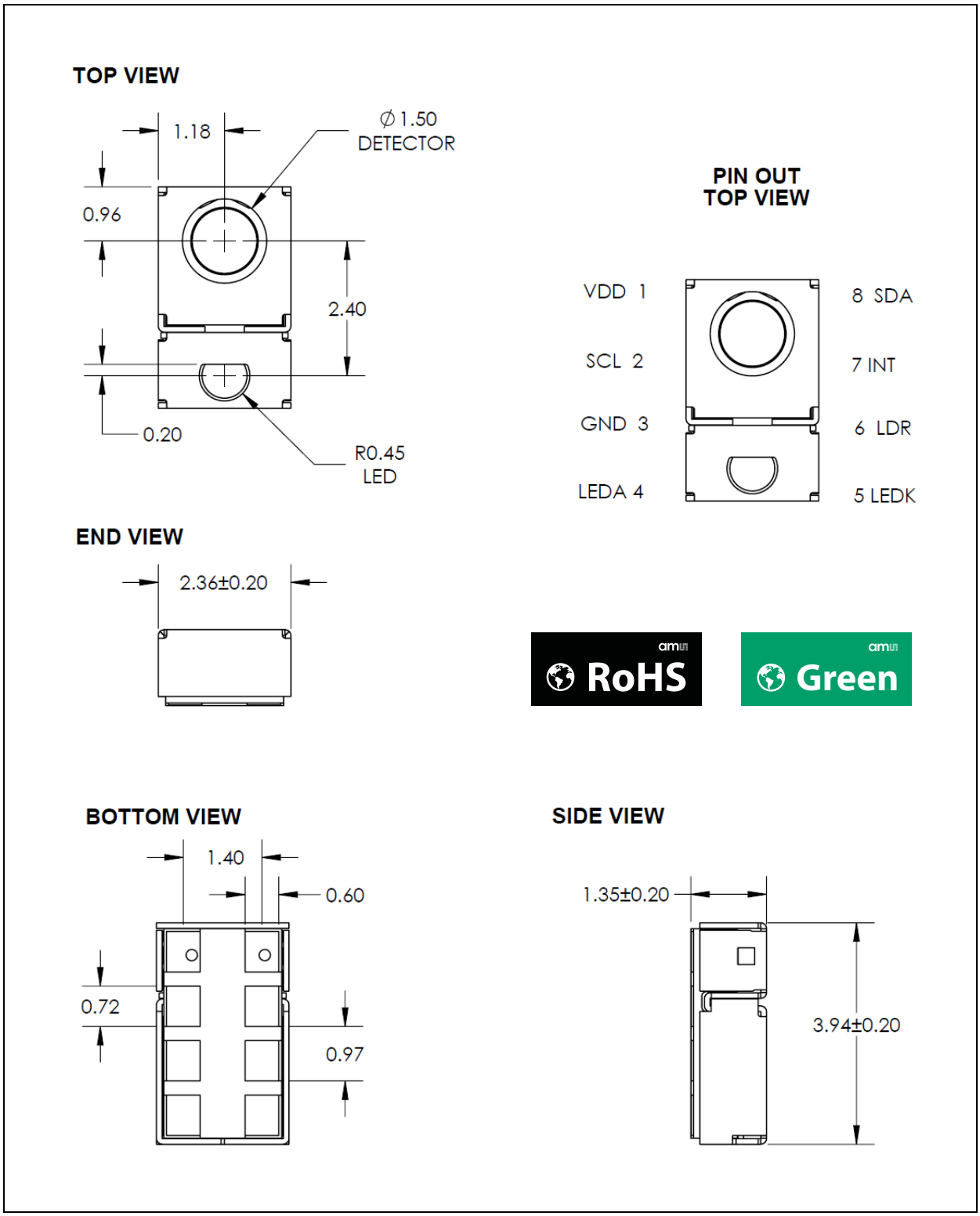
Figure 52:
TMD2772 Module Dimensions



Note(s):

1. All linear dimensions are in millimeters.
2. Dimension tolerance is ± 0.05 mm unless otherwise noted.
3. Contacts are copper with NiPdAu plating.
4. This package contains no lead (Pb).
5. This drawing is subject to change without notice.

Figure 53:
TMD2772WA Module Dimensions

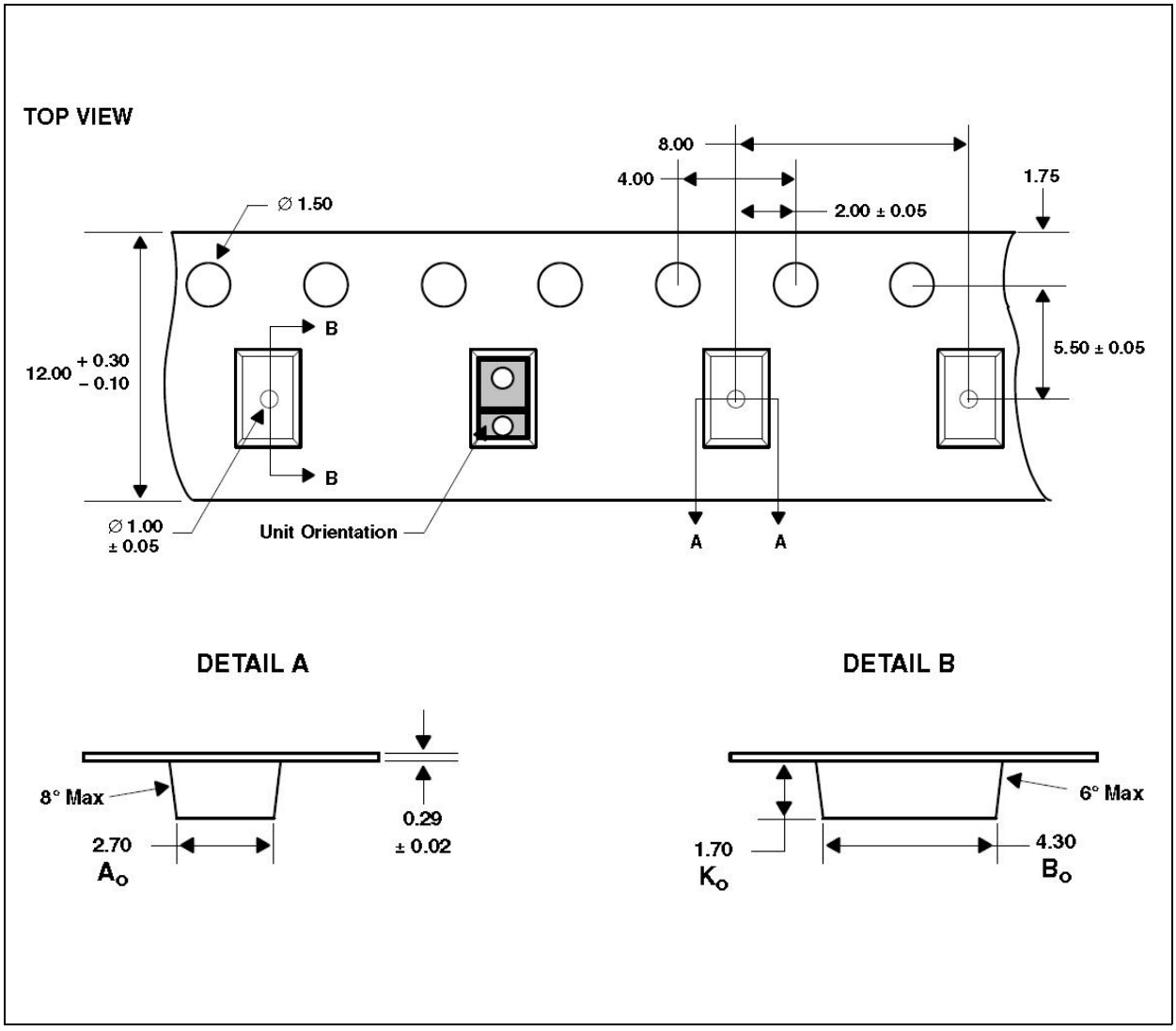


Note(s):

1. All linear dimensions are in millimeters.
2. Dimension tolerance is ± 0.05 mm unless otherwise noted.
3. Contacts are copper with NiPdAu plating.
4. This package contains no lead (Pb).
5. This drawing is subject to change without notice.

Carrier Tape & Reel Information

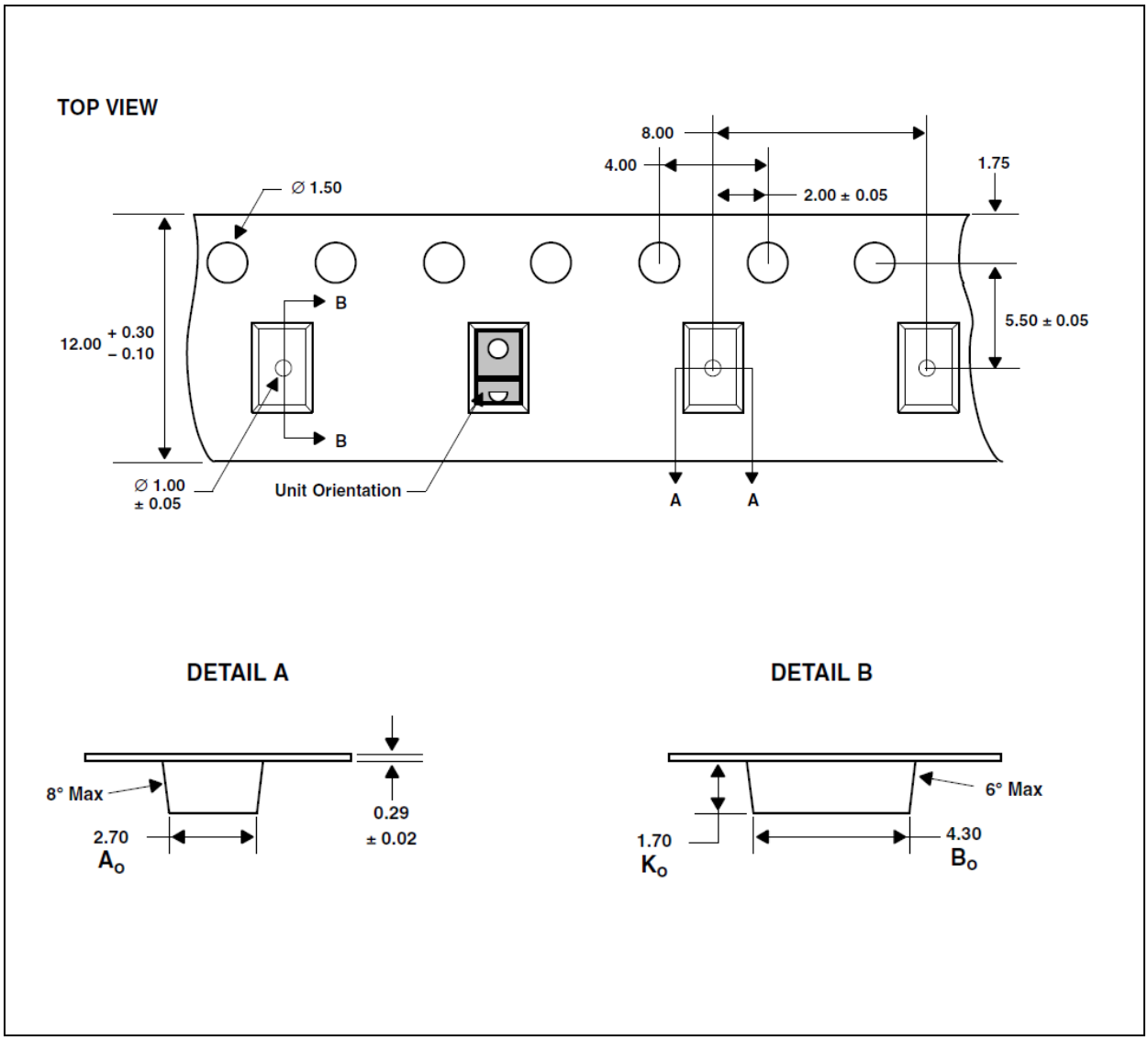
Figure 54:
TMD2772 Module Carrier Tape



Note(s):

1. All linear dimensions are in millimeters. Dimension tolerance is ± 0.10mm unless otherwise noted.
2. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
3. Symbols on drawing A_o, B_o, and K_o are defined in ANSI EIA Standard 481–B 2001.
4. Each reel is 330 millimeters in diameter and contains 2500 parts.
5. **ams** packaging tape and reel conform to the requirements of EIA Standard 481–B.
6. In accordance with EIA standard, device pin 1 is located next to the sprocket holes in the tape.
7. This drawing is subject to change without notice.

Figure 55:
TMD2772WA Module Carrier Tape



Note(s):

1. All linear dimensions are in millimeters. Dimension tolerance is ± 0.10mm unless otherwise noted.
2. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
3. Symbols on drawing A_o, B_o, and K_o are defined in ANSI EIA Standard 481–B 2001.
4. Each reel is 330 millimeters in diameter and contains 2500 parts.
5. **ams** packaging tape and reel conform to the requirements of EIA Standard 481–B.
6. In accordance with EIA standard, device pin 1 is located next to the sprocket holes in the tape.
7. This drawing is subject to change without notice.

Manufacturing Information

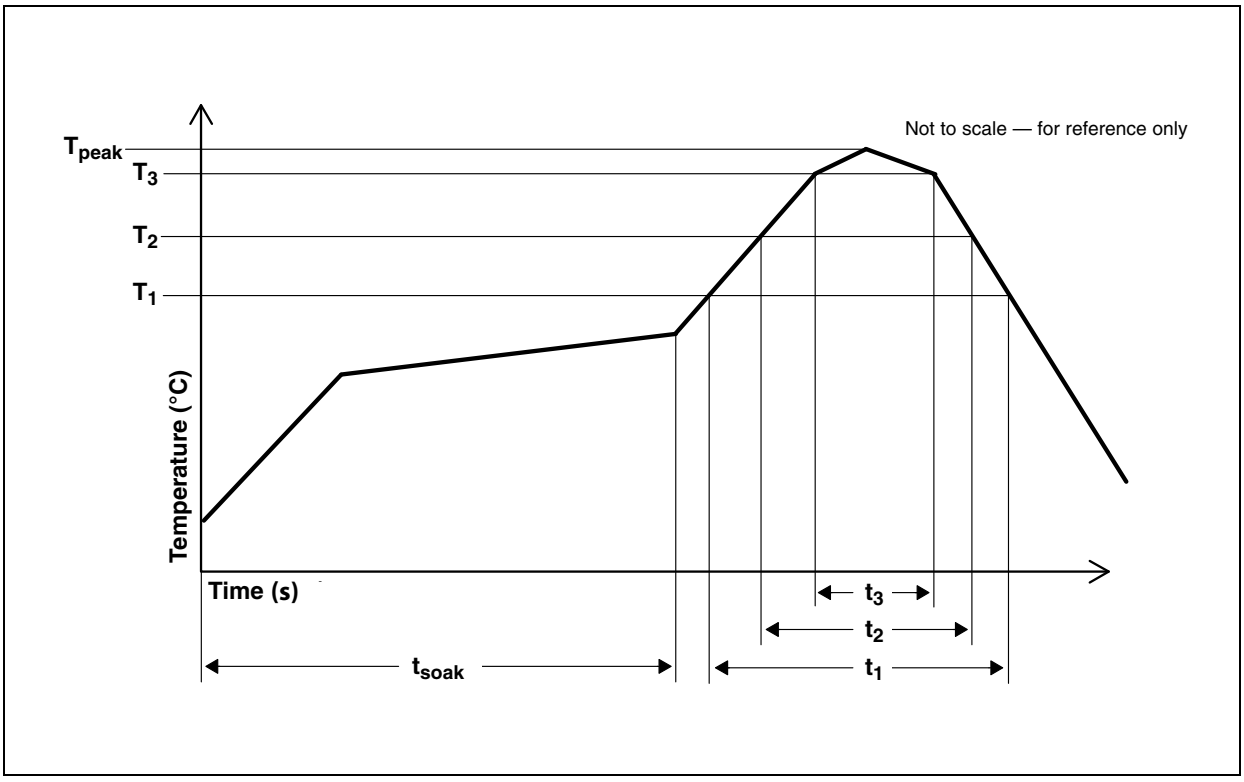
The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate.

The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Figure 56:
Solder Reflow Profile

Parameter	Reference	Device
Average temperature gradient in preheating		2.5°C/s
Soak time	t_{soak}	2 to 3 minutes
Time above 217°C (T_1)	t_1	Max 60 s
Time above 230°C (T_2)	t_2	Max 50 s
Time above 250°C (T_3)	t_3	Max 10 s
Peak temperature in reflow	T_{peak}	260°C
Temperature gradient in cooling		Max –5°C/s

Figure 57:
Solder Reflow Profile Graph



Storage Information

Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping. Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 12 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 12 months
- Ambient Temperature: < 40°C
- Relative Humidity: < 90%

Rebaking of the devices will be required if the devices exceed the 12 month shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

Floor Life

The module has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor Life: 168 hours
- Ambient Temperature: ≤ 30°C
- Relative Humidity: < 60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

Ordering & Contact Information

Figure 58:
Configuration and Ordering Information

Ordering Code	Description	Package – Leads	ID (0x12)	I²C Address	Angular Response
TMD27721	I^2C $V_{BUS} = V_{DD}$ Interface	Module – 8	0x30	0x39	± 25°
TMD27723	I^2C V_{BUS} = 1.8V Interface	Module – 8	0x39	0x39	± 25°
TMD27725 (1)	I^2C $V_{BUS} = V_{DD}$ Interface	Module – 8	0x30	0x29	± 25°
TMD27727 (1)	I^2C V_{BUS} = 1.8V Interface	Module – 8	0x39	0x29	± 25°
TMD27721WA (1)	I^2C $V_{BUS} = V_{DD}$ Interface	Module – 8	0x30	0x39	± 50°
TMD27723WA	I^2C V_{BUS} = 1.8V Interface	Module – 8	0x39	0x39	± 50°

Note(s):

1. Contact **ams** for availability.

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Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
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Revision Information

Changes from 1-20 (2014-Jul-21) to current revision 1-21 (2016-Feb-16)	Page
Updated Figure 5	5
Updated Figure 58	53

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

Content Guide