AK4649VN

24bit Stereo CODEC with MIC/SPK-AMP

GENERAL DESCRIPTION

The AK4649VN features a stereo CODEC with a built-in Microphone-Amplifier and Speaker-Amplifier. Input circuits include a Microphone-Amplifier and an ALC (Automatic Level Control) circuit, and Output circuits include a Speaker-Amplifier. These circuits are suitable for portable application with recording/playback function. The AK4649VN is available in 32pin QFN(5x5mm 0.5mm pitch) utilizing less board space than competitive offerings.

FEATURES

1. Recording Function
- **Stereo Single-ended input with two Selectors**
- **MIC Amplifier**
  (+29dB/+26dB/+23dB/+20dB/+16dB/+12dB/+9dB/+6dB/+3dB/0dB)
- **Digital ALC (Automatic Level Control)**
  - **Setting Range: +36dB ~ –54dB, 0.375dB Step**
  - **Noise Suppression**
- **ADC Performance: S/(N+D): 80dB, DR, S/N: 89dB (MIC-Amp=+20dB, AVDD=3.3V)**
  S/(N+D): 80dB, DR, S/N: 100dB (MIC-Amp=0dB, AVDD=3.3V)
- **Wind-noise Reduction Filter**
- **5 Band Notch Filter**
- **Stereo Separation Emphasis**
- **Digital MIC Interface**

2. Playback Function
- **Digital De-emphasis Filter (tc=50/15μs, fs=32kHz, 44.1kHz, 48kHz)**
- **Digital ALC (Automatic Level Control)**
  - **Setting Range: +36dB ~ –54dB, 0.375dB Step**
  - **Noise Suppression**
- **Digital Volume Control:**
  - 0dB ~ –18dB, 6dB Step & 256 Linear Step (+0dB ~ - 48.13dB & Mute)
- **Stereo Separation Emphasis**
- **Stereo Line Output**
  - S/(N+D): 87dB, S/N: 97dB
- **Mono Speaker-Amp**
  - **SPK-AMP Performance: S/(N+D): 60dB@150mW, S/N: 98dB**
  - **BTL Output**
  - **Output Power: 400mW@8Ω (SVDD=3.3V)**
- **Analog Mixing: Mono Input**

3. Power Management

4. Master Clock:

(1) PLL Mode
- **Frequencies: 11.2896MHz, 12MHz, 13.5MHz, 24MHz, 27MHz (MCKI pin)**
  1fs (LRCK pin)
  32fs or 64fs (BICK pin)

(2) External Clock Mode
- **Frequencies: 256fs, 512fs or 1024fs (MCKI pin)**

5. Output Master Clock Frequencies: 32fs/64fs/128fs/256fs
- **PLL Slave Mode (LRCK pin): 7.35kHz ~ 48kHz**
- **PLL Slave Mode (BICK pin): 7.35kHz ~ 48kHz**
- **PLL Slave Mode (MCKI pin):**
  8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz

- **PLL Master Mode:**
  8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
- **EXT Master/Slave Mode:**
  7.35kHz ~ 48kHz (256fs), 7.35kHz ~ 26kHz (512fs), 7.35kHz ~ 13kHz (1024fs)

6. **μP I/F: 3-wire Serial, I²C Bus (Ver 1.0, 400kHz Fast-Mode)**
7. **Master/Slave mode**
8. **Audio Interface Format: MSB First, 2's complement**
   - **ADC: 24bit MSB justified, 16/24bit I²S**
   - **DAC: 24bit MSB justified, 16bit LSB justified, 24bit LSB justified, 16/24bit I²S**
9. **Ta = –40 ~ 85°C**
10. **Power Supply:**
    - **Analog Power Supply (AVDD): 3.0 ~ 3.6V**
    - **Digital Power Supply (DVDD): 3.0 ~ 3.6V**
    - **Speaker Power Supply (SVDD): 3.0 ~ 3.6V**
11. **Package : 32pin QFN, 5x5mm, 0.5mm pitch**
12. **Register Compatible with the AK4646**

■ Block Diagram

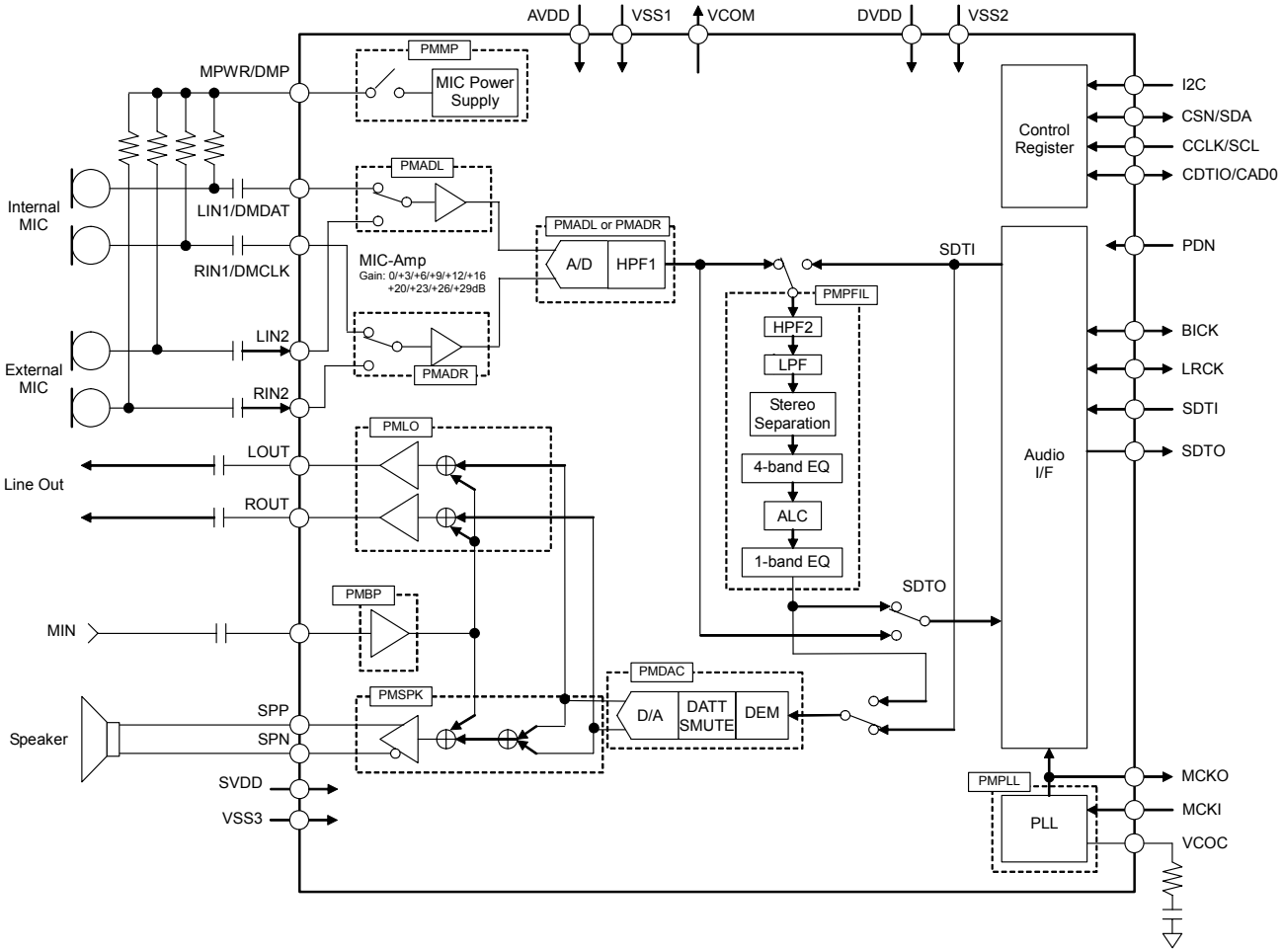
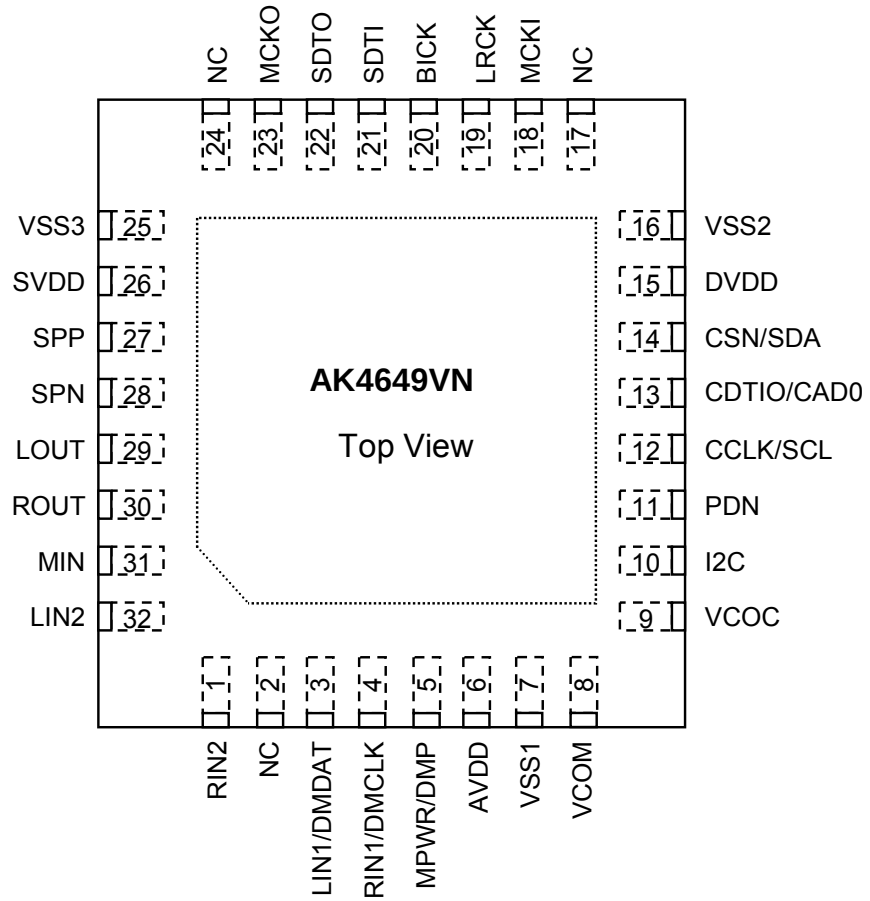


Figure 1. Block Diagram

■ Ordering Guide

AK4649VN	–40 ~ +85°C	32 pin QFN (0.5mm pitch)
AKD4649	Evaluation board for AK4649VN	

■ Pin Layout



Top View

PIN/FUNCTION

No	Pin Name	I/O	Function
1	RIN2	I	Rch Analog Input 2 Pin
2	NC	-	No Connection. No internal bonding. This pin must be connected to the ground.
3	LIN1	I	Lch Analog Input Line Input 1Pin (DMIC bit = "0")
	DMDAT	I	Digital Microphone Data Input Pin (DMIC bit = "1")
4	RIN1	I	Rch Analog Input 1 Pin (DMIC bit = "0")
	DMCLK	O	Digital Microphone Clock pin (DMIC bit = "1")
5	MPWR	O	MIC Power Supply Pin for Microphone (MPDMP bit = 0")
	DMP	O	MIC Power Supply pin for Digital Microphone (MPDMP bit = "1")
6	AVDD	-	Analog Power Supply Pin This pin must be connected to VSS1 with a 0.1μF ceramic capacitor in series.
7	VSS1	-	Ground 1 Pin
8	VCOM	O	Common Voltage Output Pin Bias voltage of ADC inputs and DAC outputs.
9	VCOC	O	Output Pin for Loop Filter of PLL Circuit This pin must be connected to VSS1 with one resistor and capacitor in series.
10	I2C	I	Control Mode Select Pin "H": I^2C Bus, "L": 3-wire mode The input circuit of the I2C pin is operated by AVDD.
11	PDN	I	Power-down & Reset When "L", the AK4649VN is in power-down mode and is held in reset. The AK4649VN must be always reset upon power-up.
12	CCLK	I	Control Data Clock Pin (I2C pin = "L")
	SCL	I	Control Data Clock Pin (I2C pin = "H")
13	CDTIO	I/O	Control Data Input/Output Pin (I2C pin = "L")
	CAD0	I	Chip Address Select Pin (I2C pin = "H")
14	CSN	I	Chip Select Pin (I2C pin = "L")
	SDA	I/O	Control Data Input/Output Pin (I2C pin = "H")
15	DVDD	-	Digital Power Supply Pin
16	VSS2	-	Ground 2 Pin
17	NC		No Connection. No internal bonding. This pin must be connected to the ground.
18	MCKI	I	External Master Clock Input Pin
19	LRCK	I/O	Input/Output Channel Clock Pin
20	BICK	I/O	Audio Serial Data Clock Pin
21	SDTI	I	Audio Serial Data Input Pin
22	SDTO	O	Audio Serial Data Output Pin
23	MCKO	O	Master Clock Output Pin
24	NC		No Connection. No internal bonding. This pin must be connected to the ground.
25	VSS3	-	Ground 3 Pin
26	SVDD	-	Speaker Amp Power Supply Pin
27	SPP	O	Speaker Amp Positive Output Pin
28	SPN	O	Speaker Amp Negative Output Pin
29	LOUT	O	Lch Analog Output Pin
30	ROUT	O	Rch Analog Output Pin
31	MIN	I	Mono Analog Signal Input Pin
32	LIN2	I	Lch Analog Input 2 pin

Note 1. All input pins except analog input pins (MIN, LIN1, RIN1, LIN1, RIN2) must not allowed to float.

■ Handling of Unused Pin

The unused I/O pins must be processed appropriately as below.

Classification	Pin Name	Setting
Analog	MPWR/DMP, VCOC, SPN, SPP, ROUT, LOUT, MIN, RIN2, LIN2, LIN1/DMDAT, RIN1/DMCLK	These pins must be open.
Digital	MCKO	These pins must be open.
	MCKI	This pin must be connected to VSS2.

ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2=VSS3=0V; Note 2)

Parameter		Symbol	min	max	Unit
Power Supplies:	Analog	AVDD	–0.3	4.6	V
	Digital	DVDD	–0.3	4.6	V
	Speaker-Amp	SVDD	–0.3	4.6	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage (Note 4)		VINA	–0.3	AVDD+0.3	V
Digital Input Voltage (Note 5)		VIND	–0.3	DVDD+0.3	V
Ambient Temperature (powered applied)		Ta	–40	85	°C
Storage Temperature		Tstg	–65	150	°C
Maximum Power Dissipation (Note 6)		Pd1	-	390	mW

Note 2. All voltages are with respect to ground.
Note 3. VSS1, VSS2 and VSS3 must be connected to the same analog ground plane.
Note 4. MIN, LIN1, RIN1, LIN2 and RIN2 pins
Note 5. PDN, CSN, CCLK, CDTIO, SDTI, LRCK, BICK and MCKI pins
Note 6. In case that PCB wiring density is 200% over and surface wiring density is 50% over. This power is the AK4649VN internal dissipation that does not include power dissipation of an externally connected speaker.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=VSS3=0V; Note 2)

Parameter		Symbol	min	typ	max	Unit
Power Supplies (Note 7)	Analog	AVDD	3.0	3.3	3.6	V
	Digital	DVDD	3.0	3.3	3.6	V
	SPK-Amp	SVDD	3.0	3.3	3.6	V
	Difference	DVDD-AVDD	-	-	+0.6	V
		AVDD–SVDD	-	-	+0.6	V

Note 2. All voltages are with respect to ground.
Note 7. The power-up sequence between AVDD, DVDD and SVDD is not critical. The PDN pin must be "L" upon power up, and should be changed to "H" after all power supplies are supplied to avoid an internal circuit error.

*** When DVDD is powered ON and the PDN pin is "L", AVDD or SVDD can be powered OFF. However, when AVDD is powered OFF, the power supply current of DVDD at power-down mode may be increased. When the AK4649VN is changed from power down state to power ON, the PDN pin must be "H" after all power supplies are ON.**

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=SVDD=3.3V; VSS1=VSS2=VSS3=0V; fs=44.1kHz, BICK=64fs;
Signal Frequency=1kHz; 24bit Data; Measurement frequency=20Hz ~ 20kHz; unless otherwise specified)

Parameter			min	typ	max	Unit
MIC Amplifier: LIN1, RIN1, LIN2, RIN2 pins						
Input Resistance			20	30	40	kΩ
Gain	MGAIN3-0 bits = "0000"		-1	0	+1	dB
	MGAIN3-0 bits = "0001"		+19	+20	+21	dB
	MGAIN3-0 bits = "0010"		+25	+26	+27	dB
	MGAIN3-0 bits = "0100"		+8	+9	+10	dB
	MGAIN3-0 bits = "0101"		+15	+16	+17	dB
	MGAIN3-0 bits = "0110"		+22	+23	+24	dB
	MGAIN3-0 bits = "0111"		+28	+29	+30	dB
	MGAIN3-0 bits = "1000"		+2	+3	+4	dB
	MGAIN3-0 bits = "1001"		+5	+6	+7	dB
	MGAIN3-0 bits = "1010"		+11	+12	+13	dB
MIC Power Supply: MPWR pin						
Output Voltage (Note 8)			2.38	2.64	2.90	V
Load Resistance			0.5	-	-	kΩ
Load Capacitance			-	-	30	pF
ADC Analog Input Characteristics: LIN1/RIN1/LIN2/RIN2 pins → ADC → IVOL, IVOL=0dB, ALC=OFF						
Resolution			-	-	24	Bits
Input Voltage (Note 9)		(Note 10)	0.208	0.231	0.254	Vpp
		(Note 11)	2.08	2.31	2.54	Vpp
S/(N+D)	(–1dBFS)	(Note 10)	70	80	-	dBFS
		(Note 11)	-	80	-	dBFS
D-Range	(–60dBFS, A-weighted)	(Note 10)	79	89	-	dB
		(Note 11)	-	100	-	dB
S/N	(A-weighted)	(Note 10)	79	89	-	dB
		(Note 11)	-	100	-	dB
Interchannel Isolation		(Note 10)	75	90	-	dB
		(Note 11)	-	100	-	dB
Interchannel Gain Mismatch		(Note 10)	-	0	0.8	dB
		(Note 11)	-	0	0.8	dB

Note 8. Output voltage is proportional to AVDD voltage. Vout = 0.8 x AVDD (typ)
Note 9. Input voltage is proportional to AVDD voltage. Vin = 0.07 x AVDD (typ) @MGAIN3-0 bits = "0001" (+20dB),
Vin = 0.7 x AVDD (typ) @MGAIN3-0 bits = "0000" (0dB)
Note 10. MGAIN3-0 bits = "0001" (+20dB)
Note 11. MGAIN3-0 bits = "0000" (0dB)

Parameter		min	typ	max	Unit
DAC Characteristics:					
Resolution		-	-	24	Bits
Stereo Line Output Characteristics: DAC → LOUT, ROUT pins, ALC=OFF, DVOL=OVOL=DATT=0dB, LOVL1-0 bit = "00", R_L=10kΩ					
Output Voltage (Note 12)	LOVL1-0 bit = "00"	2.08	2.31	2.54	Vpp
	LOVL1-0 bit = "01"	2.62	2.91	3.20	Vpp
S/(N+D) (–3dBFS)		77	87	-	dBFS
S/N (A-weighted)		87	97	-	dB
Interchannel Isolation		85	100	-	dB
Interchannel Gain Mismatch		-	0	0.8	dB
Load Resistance		10	-	-	kΩ
Load Capacitance		-	-	30	pF
Speaker-Amp Characteristics: DAC → SPP/SPN pins, ALC=OFF, DVOL=OVOL=DATT=0dB, R_L=8Ω, BTL					
Output Voltage (Note 13)					
SPKG1-0 bits = "00", –0.5dBFS (Po=150mW)		-	3.18	-	Vpp
SPKG1-0 bits = "01", –0.5dBFS (Po=250mW)		3.20	4.00	4.80	Vpp
SPKG1-0 bits = "10", –0.5dBFS (Po=400mW)		-	1.79	-	Vrms
S/(N+D)					
SPKG1-0 bits = "00", –0.5dBFS (Po=150mW)		-	60	-	dB
SPKG1-0 bits = "01", –0.5dBFS (Po=250mW)		20	50	-	dB
SPKG1-0 bits = "10", –0.5dBFS (Po=400mW)		-	20	-	dB
S/N (A-weighted)		88	98	-	dB
Load Resistance		8	-	-	Ω
Load Capacitance		-	-	30	pF

Note 12. Output voltage is proportional to AVDD voltage. Vout = 0.7 x AVDD (typ) @LOVL1-0 bit = "00".

Note 13. Output voltage is proportional to AVDD voltage.
In case of Full-differential (DAC Input Level = 0dBFS), Vout = 1.02 x AVDD (typ) @SPKG1-0 bits = "00", 1.28 x AVDD (typ) @SPKG1-0 bits = "01", 1.62 x AVDD (typ) @ SPKG1-0 bits = "10".
The output level is calculated by assuming that output signal is no clipped. In the actual case, output signal may be clipped when DAC outputs 0dBFS signal. Therefore, DAC output level should be set to lower level by setting digital volume so that Speaker-Amp output level is not clipped.

Parameter			min	typ	max	Unit
Mono Input: MIN pin, External Resistance mode (BPM bit = "0"), External Input Resistance=33kΩ						
Maximum Input Voltage (Note 14)			-	2.31	-	Vpp
Gain (Note 15)						
	MIN → LOUT/ROUT	LOVL1-0 bit = "00"	-4.5	0	+4.5	dB
		LOVL1-0 bit = "01"	-	+2	-	dB
		LOVL1-0 bit = "10"	-	+4	-	dB
		LOVL1-0 bit = "11"	-	+6	-	dB
	MIN → SPP/SPN					
		ALC bit = "0", SPKG1-0 bits = "00"	-1.2	+3.3	+7.8	dB
		ALC bit = "0", SPKG1-0 bits = "01"	-	+5.3	-	dB
		ALC bit = "0", SPKG1-0 bits = "10"	-	+7.3	-	dB
		ALC bit = "0", SPKG1-0 bits = "11"	-	+9.3	-	dB
		ALC bit = "1", SPKG1-0 bits = "00"	-	+5.3	-	dB
		ALC bit = "1", SPKG1-0 bits = "01"	-	+7.3	-	dB
		ALC bit = "1", SPKG1-0 bits = "10"	-	+9.3	-	dB
		ALC bit = "1", SPKG1-0 bits = "11"	-	+11.3	-	dB
Mono Input: MIN pin, Internal Resistance Mode (BPM bit = "1")						
Input Resistance			23	33	43	kΩ
Maximum Input Voltage (Note 16)			-	2.31	-	Vpp
Gain						
	MIN → LOUT/ROUT	LOVL1-0 bit = "00"	-1	0	+1	dB
		LOVL1-0 bit = "01"	-	+2	-	dB
		LOVL1-0 bit = "10"	-	+4	-	dB
		LOVL1-0 bit = "11"	-	+6	-	dB
	MIN → SPP/SPN					
		ALC bit = "0", SPKG1-0 bits = "00"	+1.3	+3.3	+5.3	dB
		ALC bit = "0", SPKG1-0 bits = "01"	-	+5.3	-	dB
		ALC bit = "0", SPKG1-0 bits = "10"	-	+7.3	-	dB
		ALC bit = "0", SPKG1-0 bits = "11"	-	+9.3	-	dB
		ALC bit = "1", SPKG1-0 bits = "00"	-	+5.3	-	dB
		ALC bit = "1", SPKG1-0 bits = "01"	-	+7.3	-	dB
		ALC bit = "1", SPKG1-0 bits = "10"	-	+9.3	-	dB
		ALC bit = "1", SPKG1-0 bits = "11"	-	+11.3	-	dB

Note 14. The Maximum input voltage is in proportion to both AVDD and external input resistance (Rin). Vin = 0.7 x AVDD x Rin / 33kΩ (typ).

Note 15. The gain is in inverse proportion to external input resistance.

Note 16. The Maximum input voltage is in proportion to AVDD. Vin = 0.7 x AVDD (typ) @ BPLVL = 0dB.

Parameter			min	typ	max	Unit
Power Supplies:						
Power Up (PDN pin = "H")						
	All Circuit Power-up (Note 17)					
		AVDD+DVDD	-	12.5	19	mA
		SVDD (No Load)	-	4.0	12	mA
Power Down (PDN pin = "L") (Note 18)						
	AVDD+DVDD+SVDD		-	1	5	μA

Note 17. When PLL Master Mode (MCKI=12MHz), and PMADL = PMADR = PMDAC =PMPFIL = PMLO = PMSPK = PMVCM = PMPLL = MCKO = PMBP = PMMP = M/S bits = "1". The MPWR pin outputs 0mA. AVDD = 6.8mA (typ), DVDD = 5.7mA (typ).

Note 18. All digital input pins are fixed to DVDD or VSS2.

FILTER CHARACTERISTICS

(Ta =25°C; AVDD=SVDD=3.0 ~ 3.6V, DVDD =3.0 ~ 3.6V; fs=44.1kHz; DEM=OFF)

Parameter		Symbol	min	typ	max	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 19)	±0.16dB	PB	0	-	17.3	kHz
	–0.66dB		-	19.4	-	kHz
	–1.1dB		-	19.9	-	kHz
	–6.9dB		-	22.1	-	kHz
Stopband		SB	26.1	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	73	-	-	dB
Group Delay (Note 20)		GD	-	19	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
ADC Digital Filter (HPF): HPFC1-0 bits = "00"						
Frequency Response	–3.0dB	FR	-	3.4	-	Hz
	–0.5dB		-	10	-	Hz
	–0.1dB		-	22	-	Hz
DAC Digital Filter (LPF):						
Passband (Note 19)	±0.05dB	PB	0	-	20.0	kHz
	–6.0dB		-	22.05	-	kHz
Stopband		SB	24.1	-	-	kHz
Passband Ripple		PR	-	-	±0.02	dB
Stopband Attenuation		SA	54	-	-	dB
Group Delay (Note 20)		GD	-	20	-	1/fs
DAC Digital Filter (LPF) + SCF:						
Frequency Response: 0 ~ 20.0kHz		FR	-	±1.0	-	dB

Note 19. The passband and stopband frequencies scale with fs (system sampling rate).
For example, PB=20.0kHz (@–1.0dB) is 0.454 x fs (ADC). Each response refers to that of 1kHz

Note 20. The calculated delay time caused by digital filtering. This time is from the input of analog signal to setting of the 24-bit data of both channels from the input register to the output register of the ADC. This time includes the group delay of the HPF. For the DAC, this time is from setting the 24-bit data of both channels from the input register to the output of analog signal.
For the signal through the programmable filters (First HPF + First LPF + 4-band Equalizer + ALC + Equalizer), group delay is increased 5/fs at Recording Mode or 7/fs at Playback Mode from the value above if there is no phase change by the IIR filter.

DC CHARACTERISTICS

(Ta = 25°C; AVDD=SVDD=3.0 ~ 3.6V, DVDD =3.0 ~ 3.6V; fs=44.1kHz)

Parameter	Symbol	min	typ	max	Unit
Audio Interface & Serial µP Interface (CDTIO/CAD0, CSN/SDA, CCLK/SCL, I2C, PDN, BICK, LRCK, SDTI, MCKI pins)					
High-Level Input Voltage	VIH	70%DVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%DVDD	V
Audio Interface & Serial µP Interface (CDTIO, SDA MCKO, BICK, LRCK, SDTO pins Output)					
High-Level Output Voltage (Iout = −80µA)	VOH	DVDD−0.2	-	-	V
Low-Level Output Voltage					
(Except SDA pin : Iout = 80µA)	VOL1	-	-	0.2	V
(SDA pin : Iout = 3mA)	VOL2	-	-	0.4	V
Input Leakage Current	Iin	-	-	±10	µA
Digital MIC Interface (DMDAT pin Input ; DMIC bit = "1")					
High-Level Input Voltage	VIH3	65%AVDD	-	-	V
Low-Level Input Voltage	VIL3	-	-	35%AVDD	V
Digital MIC Interface (DMCLK pin Output ; DMIC bit = "1")					
High-Level Output Voltage (Iout=−80µA)	VOH3	AVDD-0.4	-	-	V
Low-Level Output Voltage (Iout= 80µA)	VOL3	-	-	0.4	V
Input Leakage Current	Iin	-	-	±10	µA

SWITCHING CHARACTERISTICS

(Ta = 25°C; AVDD=SVDD=3.0 ~ 3.6V, DVDD =3.0 ~ 3.6V; C_L=20pF)

Parameter		Symbol	min	typ	max	Unit
PLL Master Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency		fCLK	11.2896	-	27	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
MCKO Output Timing						
Frequency		fMCK	0.2352	-	12.288	MHz
Duty Cycle						
Except 256fs at fs=32kHz, 29.4kHz		dMCK	40	50	60	%
256fs at fs=32kHz, 29.4kHz		dMCK	-	33	-	%
LRCK Output Timing						
Frequency		fs	7.35	-	48	kHz
Duty Cycle		Duty	-	50	-	%
BICK Output Timing						
Period	BCKO bit = "0"	tBCK	-	1/(32fs)	-	ns
	BCKO bit = "1"	tBCK	-	1/(64fs)	-	ns
Duty Cycle		dBCK	-	50	-	%
PLL Slave Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency		fCLK	11.2896	-	27	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
MCKO Output Timing						
Frequency		fMCK	0.2352	-	12.288	MHz
Duty Cycle						
Except 256fs at fs=32kHz, 29.4kHz		dMCK	40	50	60	%
256fs at fs=32kHz, 29.4kHz		dMCK	-	33	-	%
LRCK Input Timing						
Frequency		fs	7.35	-	48	kHz
Duty		Duty	45	-	55	%
BICK Input Timing						
Period		tBCK	1/(64fs)	-	1/(32fs)	ns
Pulse Width Low		tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High		tBCKH	0.4 x tBCK	-	-	ns

Parameter			Symbol	min	typ	max	Unit
PLL Slave Mode (PLL Reference Clock = LRCK pin)							
LRCK Input Timing							
Frequency			fs	7.35	-	48	kHz
Duty			Duty	45	-	55	%
BICK Input Timing							
Period			tBCK	1/(64fs)	-	1/(32fs)	ns
Pulse Width Low			tBCKL	240	-	-	ns
Pulse Width High			tBCKH	240	-	-	ns
PLL Slave Mode (PLL Reference Clock = BICK pin)							
LRCK Input Timing							
Frequency			fs	7.35	-	48	kHz
Duty			Duty	45	-	55	%
BICK Input Timing							
Period	PLL3-0 bits = “0010”		tBCK	-	1/(32fs)	-	ns
	PLL3-0 bits = “0011”		tBCK	-	1/(64fs)	-	ns
Pulse Width Low			tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High			tBCKH	0.4 x tBCK	-	-	ns
External Slave Mode							
MCKI Input Timing							
Frequency	256fs		fCLK	1.8816	-	12.288	MHz
	512fs		fCLK	3.7632	-	13.312	MHz
	1024fs		fCLK	7.5264	-	13.312	MHz
Pulse Width Low			tCLKL	0.4/fCLK	-	-	ns
Pulse Width High			tCLKH	0.4/fCLK	-	-	ns
LRCK Input Timing							
Frequency	256fs		fs	7.35	-	48	kHz
	512fs		fs	7.35	-	26	kHz
	1024fs		fs	7.35	-	13	kHz
Duty			Duty	45	-	55	%
BICK Input Timing							
Period			tBCK	312.5	-	-	ns
Pulse Width Low			tBCKL	130	-	-	ns
Pulse Width High			tBCKH	130	-	-	ns
External Master Mode							
MCKI Input Timing							
Frequency	256fs		fCLK	1.8816	-	12.288	MHz
	512fs		fCLK	3.7632	-	13.312	MHz
	1024fs		fCLK	7.5264	-	13.312	MHz
Pulse Width Low			tCLKL	0.4/fCLK	-	-	ns
Pulse Width High			tCLKH	0.4/fCLK	-	-	ns
LRCK Output Timing							
Frequency			fs	7.35	-	48	kHz
Duty Cycle			Duty	-	50	-	%
BICK Output Timing							
Period		BCKO bit = “0”	tBCK	-	1/(32fs)	-	ns
		BCKO bit = “1”	tBCK	-	1/(64fs)	-	ns
Duty Cycle			dBCK	-	50	-	%

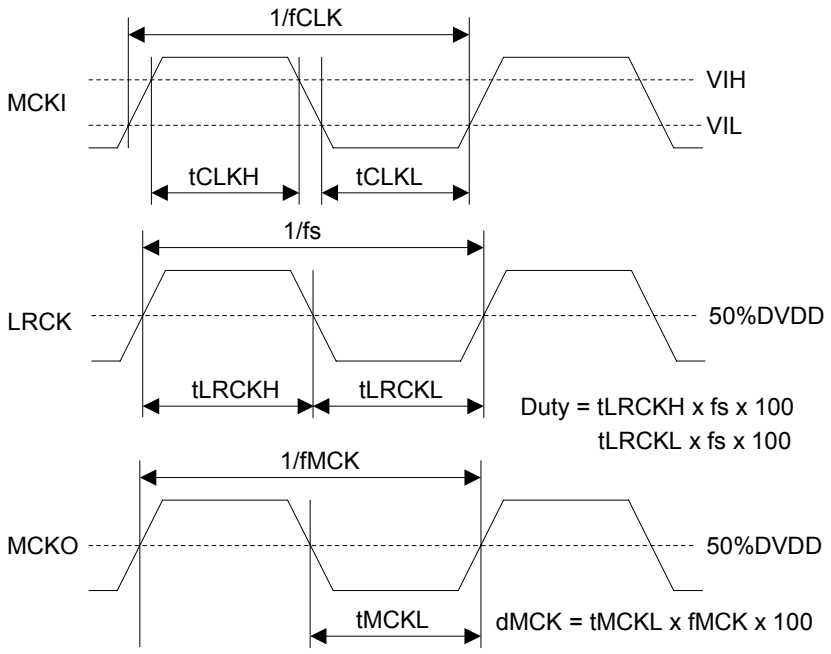
Parameter	Symbol	min	typ	max	Unit
Audio Interface Timing					
Master Mode					
BICK "↓" to LRCK Edge (Note 21)	tMBLR	–40	-	40	ns
LRCK Edge to SDTO (MSB) (Except I²S mode)	tLRD	–70	-	70	ns
BICK "↓" to SDTO	tBSD	–70	-	70	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Slave Mode					
LRCK Edge to BICK "↑" (Note 21)	tLRB	50	-	-	ns
BICK "↑" to LRCK Edge (Note 21)	tBLR	50	-	-	ns
LRCK Edge to SDTO (MSB) (Except I²S mode)	tLRD	-	-	80	ns
BICK "↓" to SDTO	tBSD	-	-	80	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Control Interface Timing (3-wire Mode):					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
Pulse Width High	tCCKH	80	-	-	ns
CDTIO Setup Time	tCDS	40	-	-	ns
CDTIO Hold Time	tCDH	40	-	-	ns
CSN "H" Time	tCSW	150	-	-	ns
CSN Edge to CCLK "↑" (Note 22)	tCSS	50	-	-	ns
CCLK "↑" to CSN Edge (Note 22)	tCSH	50	-	-	ns
CCLK "↓" to CDTIO (at Read Command)	tDCD	-	-	70	ns
CSN "↑" to CDTIO (Hi-Z) (at Read Command)(Note 24)	tCCZ	-	-	70	ns
Control Interface Timing (I²C Bus Mode):					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling (Note 25)	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Capacitive Load on Bus	Cb	-	-	400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns

Note 21. BICK rising edge must not occur at the same time as LRCK edge.
Note 22. CCLK rising edge must not occur at the same time as CSN edge.
Note 23. I²C-bus is a trademark of NXP B.V.
Note 24. R_L=1kΩ/10% change (pull-up or DVDD)
Note 25. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

Parameter	Symbol	min	typ	max	Unit
Digital Audio Interface Timing; C_L=100pF					
DMCLK Output Timing					
Period	tSCK	-	1/(64fs)	-	ns
Rising Time	tSRise	-	-	10	ns
Falling Time	tSFall	-	-	10	ns
Duty Cycle	dSCK	40	50	60	%
Audio Interface Timing					
DMDAT Setup Time	tSDS	50	-	-	ns
DMDAT Hold Time	tSDH	0	-	-	ns
Power-down & Reset Timing					
PDN Pulse Width (Note 26)	tPD	150	-	-	ns
PMADL or PMADR "↑" to SDTO valid (Note 27)					
ADRST bit = "0"	tPDV	-	1059	-	1/fs
ADRST bit = "1"	tPDV	-	267	-	1/fs

Note 26. The AK4649VN can be reset by the PDN pin = "L".
Note 27. This is the count of LRCK "↑" from the PMADL or PMADR bit = "1".

■ Timing Diagram



Note 28. MCKO is not available at EXT Master mode.
Figure 2. Clock Timing (PLL/EXT Master mode)

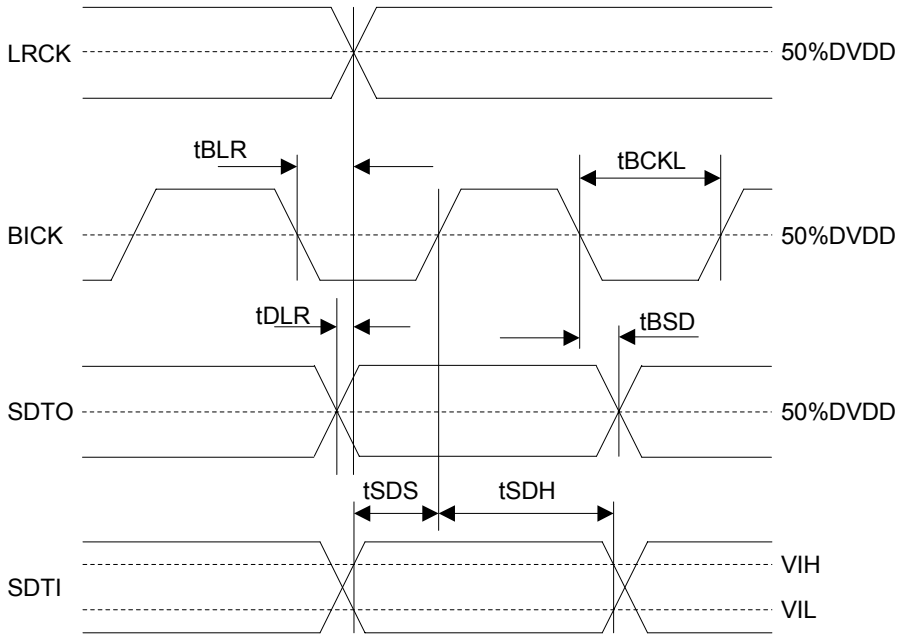


Figure 3. Audio Interface Timing (PLL/EXT Master mode)

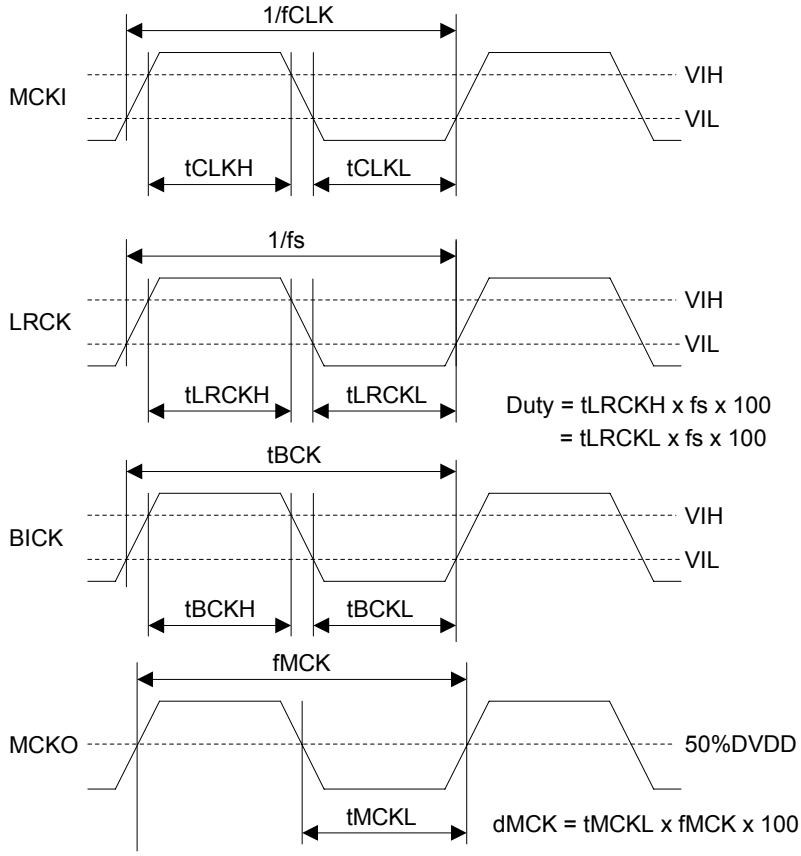


Figure 4. Clock Timing (PLL Slave mode; PLL Reference Clock = MCKI pin)

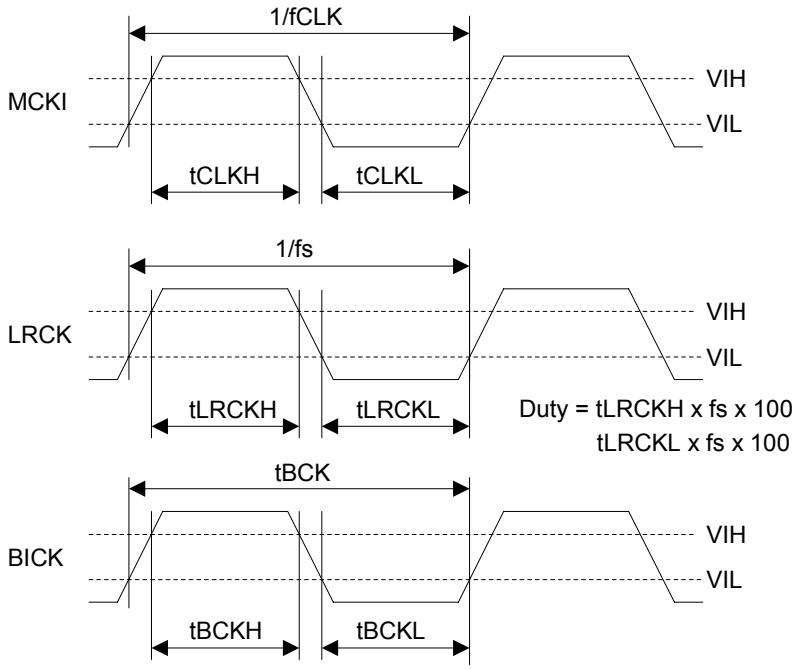


Figure 5. Clock Timing (EXT Slave mode)

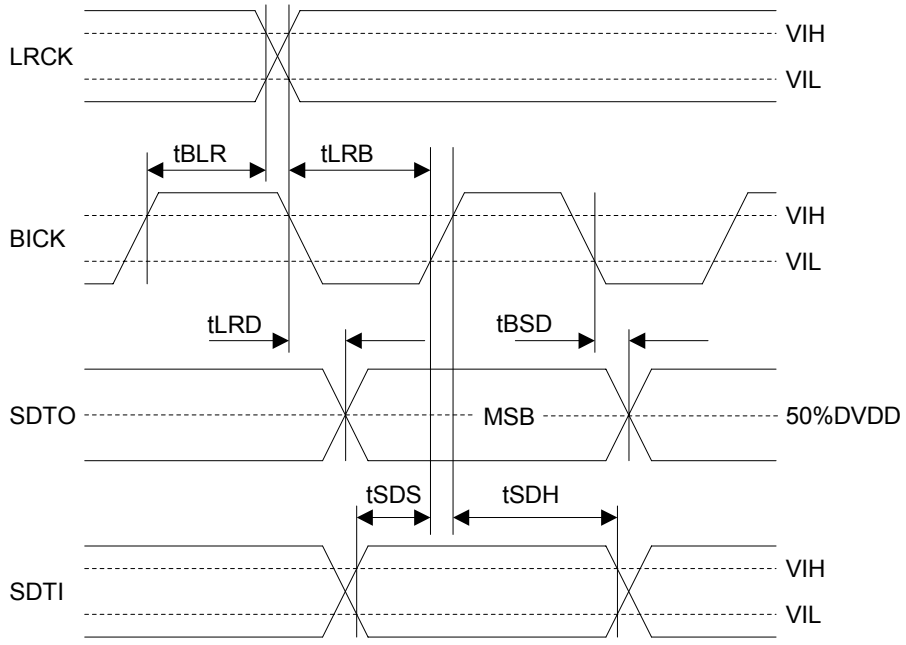


Figure 6. Audio Interface Timing (PLL/EXT Slave mode)

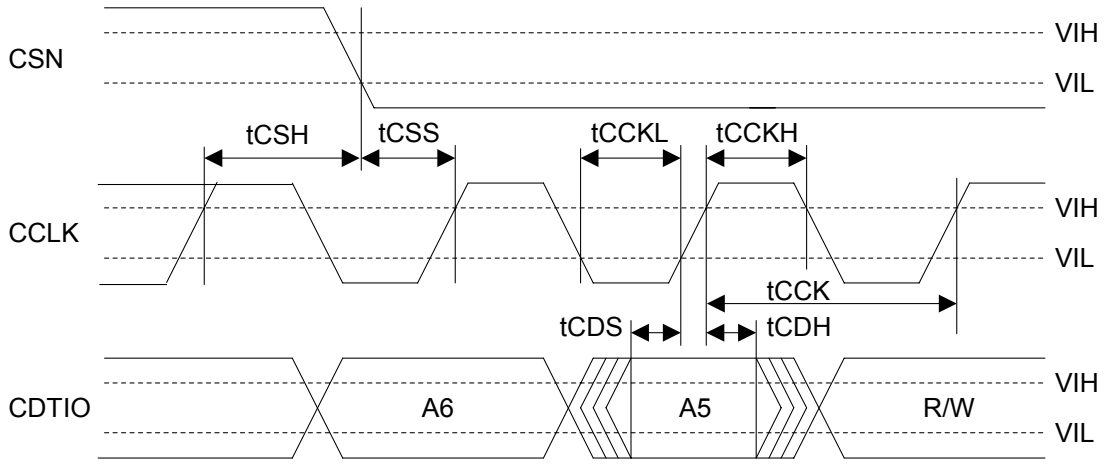


Figure 7. WRITE Command Input Timing

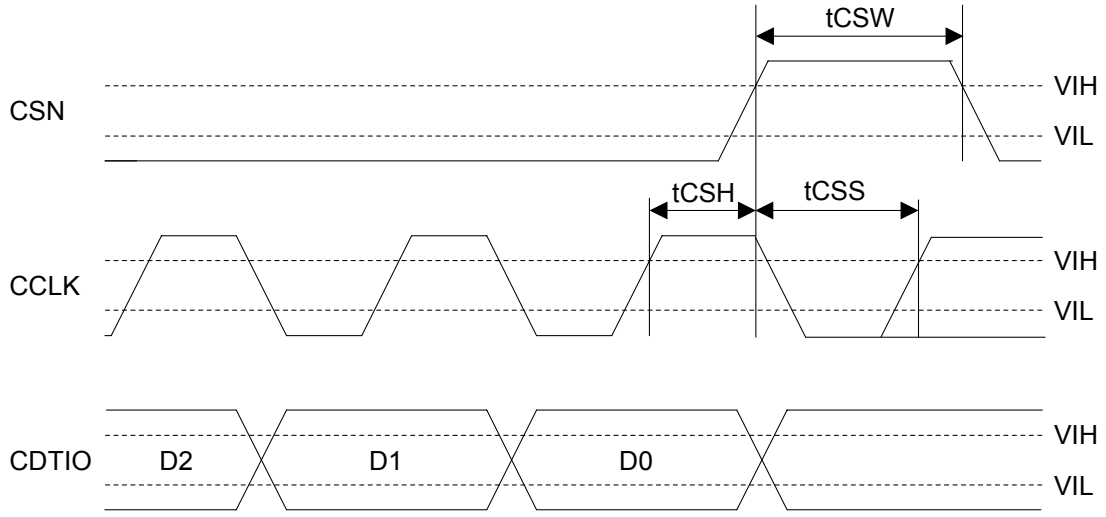


Figure 8. WRITE Data Input Timing

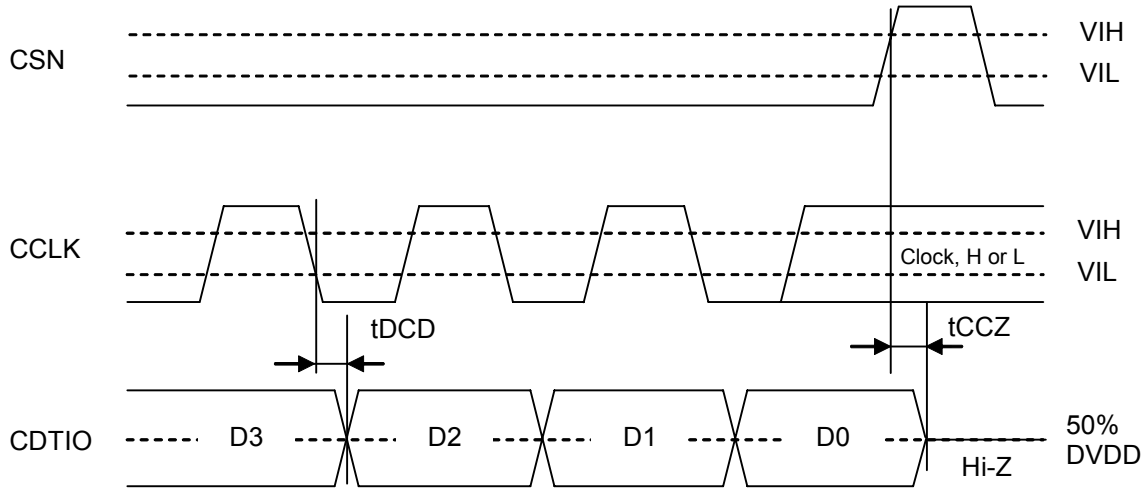


Figure 9. Read Data Output Timing

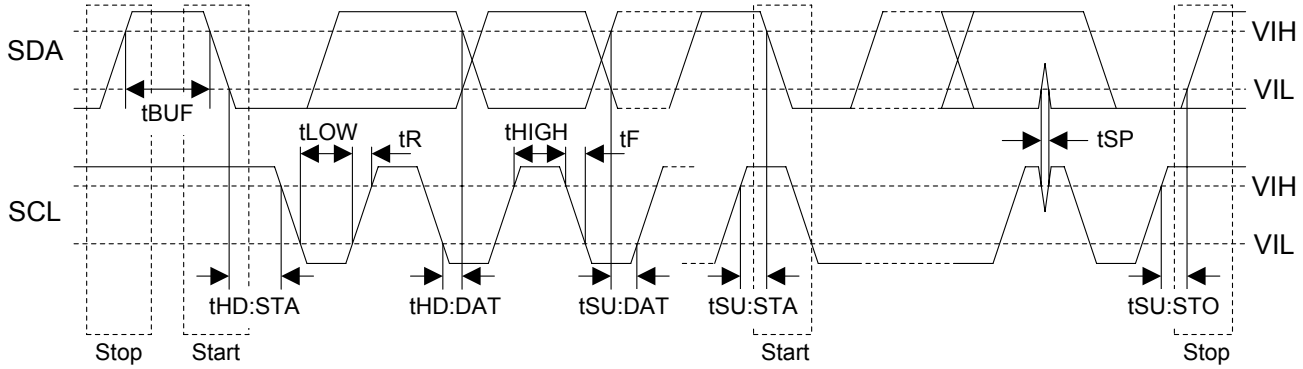


Figure 10. I^{2}C Bus Mode Timing

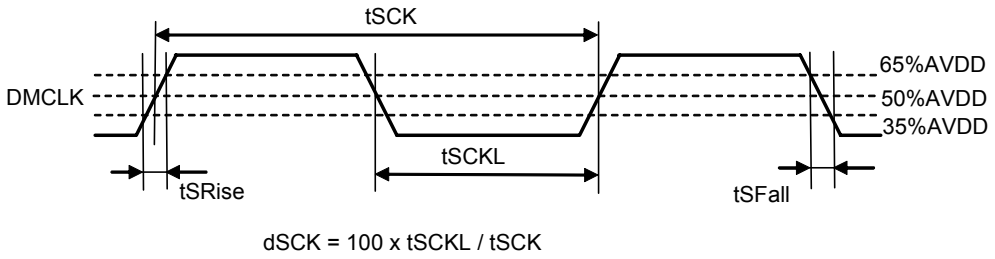


Figure 11. DMCLK Clock Timing

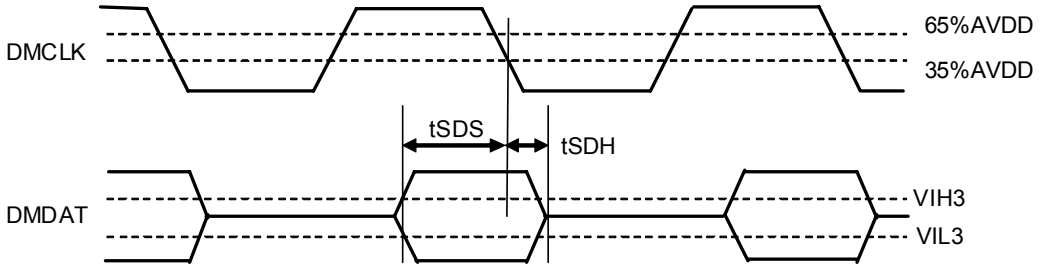


Figure 30. Audio Interface Timing (DCLKP bit = "1")

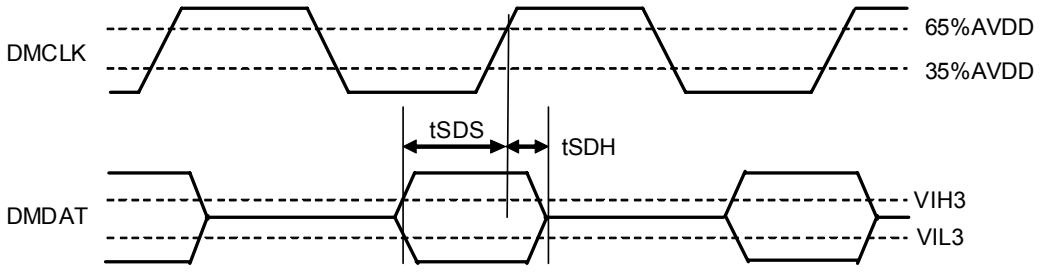


Figure 31. Audio Interface Timing (DCLKP bit = "0")

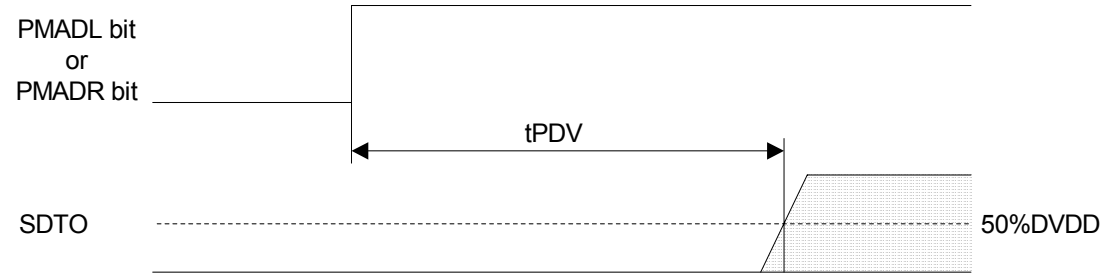


Figure 12. Power Down & Reset Timing 1

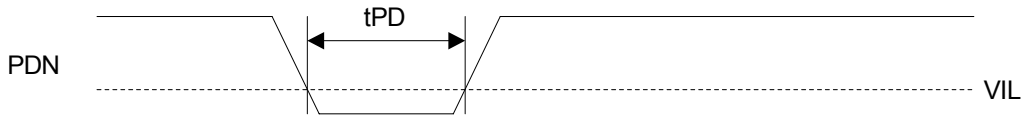


Figure 13. Power Down & Reset Timing 2

OPERATION OVERVIEW

■ System Clock

There are the following five clock modes to interface with external devices (Table 1, Table 2).

Mode	PMPLL bit	M/S bit	PLL3-0 bits	Figure
PLL Master Mode (Note 29)	1	1	Table 4	Figure 14
PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)	1	0	Table 4	Figure 15
PLL Slave Mode 2 (PLL Reference Clock: LRCK or BICK pin)	1	0	Table 4	Figure 16 Figure 17
EXT Slave Mode	0	0	x	Figure 18
EXT Master Mode	0	1	x	Figure 19

Note 29. If M/S bit = "1", PMPLL bit = "0" and MCKO bit = "1" during the setting of PLL Master Mode, the invalid clocks are output from the MCKO pin.

Table 1. Clock Mode Setting (x: Don't care)

Mode	MCKO bit	MCKO pin	MCKI pin	BICK pin	LRCK pin
PLL Master Mode	0	L	Selected by PLL3-0 bits	Output (Selected by BCKO bit)	Output (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode (PLL Reference Clock: MCKI pin)	0	L	Selected by PLL3-0 bits	Input (Selected by BCKO bit)	Input (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode (PLL Reference Clock: LRCK or BICK pin)	0	L	GND	Input (Selected by BCKO bit)	Input (1fs)
EXT Slave Mode	0	L	Selected by PLL3-0 bits	Input (≥ 32fs)	Input (1fs)
EXT Master Mode	0	L	Selected by PLL3-0 bits	Output (Selected by BCKO bit)	Output (1fs)

Note 30. When PMVCM bit = M/S bit = "1" and MCKI is input, LRCK and BICK are output, even if PMDAC bit = PMADL bit = PMADR bit = "0".

Table 2. Clock pins state in Clock Mode

■ Master Mode/Slave Mode

The M/S bit selects either master or slave mode. M/S bit = "1" selects master mode and "0" selects slave mode. When the AK4649VN is power-down mode (PDN pin = "L") and exits reset state, the AK4649VN is in slave mode. After exiting reset state, the AK4649VN goes to master mode by changing M/S bit = "1".

When the AK4649VN is in master mode, the LRCK and BICK pins are a floating state until M/S bit becomes "1". The LRCK and BICK pins of the AK4649VN must be pulled-down or pulled-up by the resistor (about 100kΩ) externally to avoid the floating state.

M/S bit	Mode	
0	Slave Mode	(default)
1	Master Mode	

Table 3. Select Master/Slave Mode

■ PLL Mode

When PMPLL bit is "1", a fully integrated analog phase locked loop (PLL) generates a clock that is selected by the PLL3-0 and FS3-0 bits. The PLL lock time is shown in Table 4, when the AK4649VN is supplied stable clocks after PLL is powered-up (PMPLL bit = "0" → "1") or when the sampling frequency is changed.

1) PLL Mode Setting

Mode	PLL3 bit	PLL2 bit	PLL1 bit	PLL0 bit	PLL Reference Clock Input Pin	Input Frequency	R and C of VCOC pin		PLL Lock Time (max)	
							R[Ω]	C[F]		
0	0	0	0	0	LRCK pin	1fs	6.8k	220n	160ms	(default)
1	0	0	0	1	N/A	-	-	-	-	
2	0	0	1	0	BICK pin	32fs	10k	4.7n	2ms	
3	0	0	1	1	BICK pin	64fs	10k	4.7n	2ms	
4	0	1	0	0	MCKI pin	11.2896MHz	10k	4.7n	10ms	
6	0	1	1	0	MCKI pin	12MHz	10k	4.7n	10ms	
7	0	1	1	1	MCKI pin	24MHz	10k	4.7n	10ms	
12	1	1	0	0	MCKI pin	13.5MHz	10k	10n	10ms	
13	1	1	0	1	MCKI pin	27MHz	10k	10n	10ms	
Others	Others				N/A					

Note 31. R has a tolerance of ± 5%, and C has a tolerance of ± 30%.

Table 4. Setting of PLL Mode (*fs: Sampling Frequency, N/A: Not Available)

2) Setting of sampling frequency in PLL Mode

When PLL2 bit is "1" (PLL reference clock input is MCKI pin), the sampling frequency is selected by FS3-0 bits as defined in Table 5.

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency	
0	0	0	0	0	8kHz	(default)
1	0	0	0	1	12kHz	
2	0	0	1	0	16kHz	
3	0	0	1	1	24kHz	
4	0	1	0	0	7.35kHz	
5	0	1	0	1	11.025kHz	
6	0	1	1	0	14.7kHz	
7	0	1	1	1	22.05kHz	
10	1	0	1	0	32kHz	
11	1	0	1	1	48kHz	
14	1	1	1	0	29.4kHz	
15	1	1	1	1	44.1kHz	
Others	Others				N/A	

Table 5. Setting of Sampling Frequency at PLL2 bit = "1" and PMPLL bit = "1" (Reference Clock = MCKI pin), (N/A: Not Available)

When PLL2 bit is "0" (PLL reference clock input is LRCK or BICK pin), the sampling frequency is selected by FS3 and FS2 bits. (Table 6).

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency Range	
0	0	0	x	x	7.35kHz ≤ fs ≤ 12kHz	(default)
1	0	1	x	x	12kHz < fs ≤ 24kHz	
2	1	0	x	x	24kHz < fs ≤ 48kHz	
Others	Others				N/A	

Table 6. Setting of Sampling Frequency at PLL2 bit = "0" and PMPLL bit = "1" PLL Slave Mode 2 (PLL Reference Clock: LRCK or BICK pin), (x: Don't care, N/A: Not Available)

■ PLL Unlock State

1) PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

In this mode, the LRCK and BICK pins go to "L" and irregular frequency clock is output from the MCKO pin at MCKO bit is "1" before the PLL goes to lock state after PMPLL bit = "0" → "1". If MCKO bit is "0", the MCKO pin goes to "L" (Table 7).

After the PLL is locked, a first period of LRCK and BICK may be invalid clock, but these clocks return to normal state after a period of 1/fs.

When sampling frequency is changed, the BICK and LRCK pins do not output irregular frequency clocks but go to "L" by setting PMPLL bit to "0".

PLL State	MCKO pin		BICK pin	LRCK pin
	MCKO bit = "0"	MCKO bit = "1"		
After PMPLL bit "0" → "1"	"L" Output	Invalid	"L" Output	"L" Output
PLL Unlock (except the case above)	"L" Output	Invalid	Invalid	Invalid
PLL Lock	"L" Output	Table 9	Table 10	1fs Output

Table 7. Clock Operation at PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

2) PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

In this mode, an invalid clock is output from the MCKO pin before the PLL goes to lock state after PMPLL bit = "0" → "1". Then, the clock selected by Table 9 is output from the MCKO pin when PLL is locked. ADC and DAC output invalid data when the PLL is unlocked. For DAC, the output signal can be muted by writing "0" to DACL and DACS bits.

PLL State	MCKO pin	
	MCKO bit = "0"	MCKO bit = "1"
After PMPLL bit "0" → "1"	"L" Output	Invalid
PLL Unlock (except the case above)	"L" Output	Invalid
PLL Lock	"L" Output	Output

Table 8. Clock Operation at PLL Slave Mode (PMPLL bit = "0", M/S bit = "0")

■ PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

When an external clock (11.2896MHz, 12MHz, 13.5MHz, 24MHz or 27MHz) is input to the MCKI pin, MCKO, BICK and LRCK clocks are generated by an internal PLL circuit. The MCKO output frequency is selected by PS1-0 bits (Table 9) and the output is enabled by MCKO bit. The BICK output frequency is selected between 32fs or 64fs, by BCKO bit (Table 10).

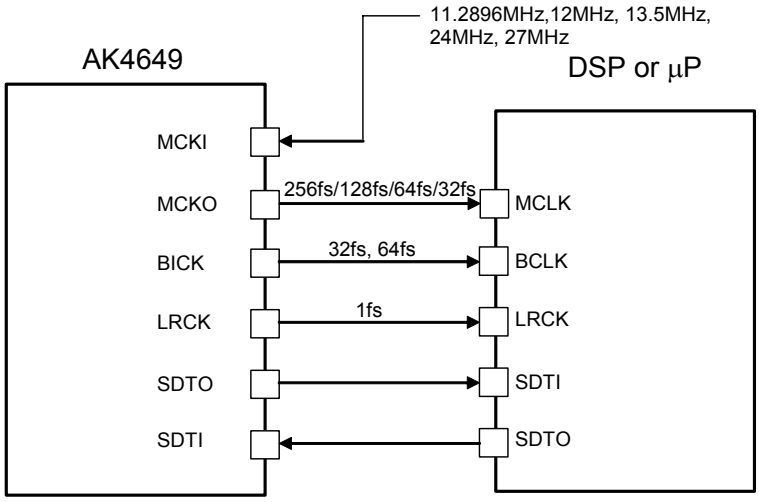


Figure 14. PLL Master Mode

Mode	PS1 bit	PS0 bit	MCKO pin	
0	0	0	256fs	(default)
1	0	1	128fs	
2	1	0	64fs	
3	1	1	32fs	

Table 9. MCKO Output Frequency (PLL Mode, MCKO bit = "1")

BCKO bit	BICK Output Frequency	
0	32fs	(default)
1	64fs	

Table 10. BICK Output Frequency at Master Mode

■ PLL Slave Mode (PMPLL bit = “1”, M/S bit = “0”)

A reference clock of PLL is selected among the input clocks to the MCKI, BICK or LRCK pin. The required clock for the AK4649VN is generated by an internal PLL circuit. Input frequency is selected by PLL3-0 bits (Table 4).

a) PLL reference clock: MCKI pin

BICK and LRCK inputs must be synchronized with MCKO output. The phase between MCKO and LRCK dose not matter. The MCKO pin outputs the frequency selected by PS1-0 bits (Table 9) and the output is enabled by MCKO bit. Sampling frequency can be selected by FS3-0 bits (Table 5)

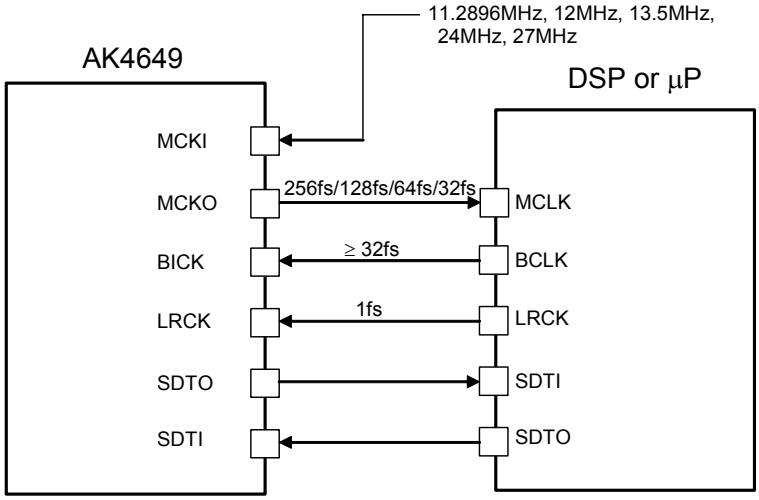


Figure 15. PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)

b) PLL reference clock: BICK or LRCK pin

Sampling frequency corresponds to 7.35kHz to 48kHz by changing FS3-0 bits (Table 6).

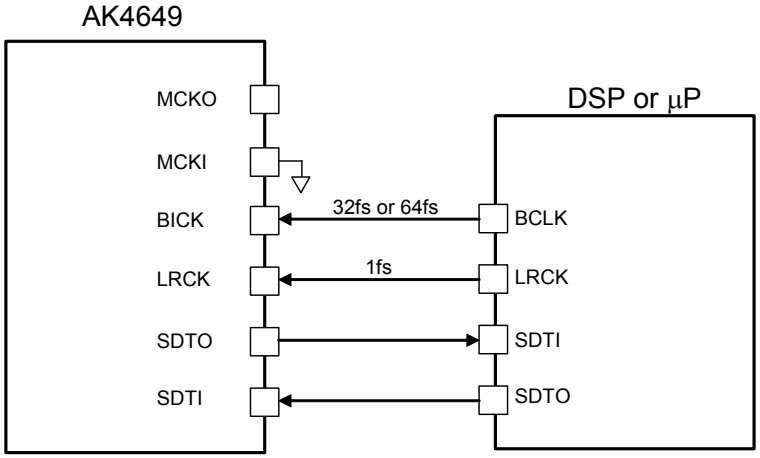


Figure 16. PLL Slave Mode 2 (PLL Reference Clock: BICK pin)

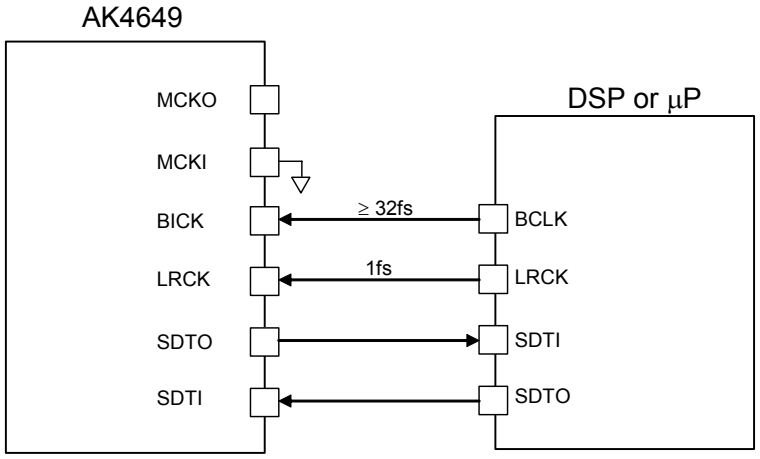


Figure 17 PLL Slave Mode 2 (PLL Reference Clock: LRCK pin)

The external clocks (MCKI, BICK and LRCK) must always be present whenever the ADC, DAC or Programmable Filter is in operation (PMADL bit = "1", PMADR bit = "1" PMDAC, or PMPFIL bit = "1"). If these clocks are not provided, the AK4649VN may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If the external clocks are not present, the ADC, DAC and Programmable Filter should be in the power-down mode (PMADL=PMADR=PMDAC =PMPFIL bits = "0").

■ EXT Slave Mode (PMPLL bit = “0”, M/S bit = “0”)

When PMPLL bit is “0”, the AK4649VN becomes EXT mode. Master clock can directly be inputted from the MCKI pin, without the internal PLL circuit operation. This mode is compatible with I/F of the normal audio CODEC. The clocks required to operate this mode are MCKI (256fs, 512fs or 1024fs), LRCK (fs) and BICK (≥32fs). The master clock (MCKI) must be synchronized with LRCK. The phase between these clocks does not matter. The input frequency of MCKI is selected by FS1-0 bits (Table 11).

Mode	FS3-2 bits	FS1 bit	FS0 bit	MCKI Input Frequency	Sampling Frequency Range	
0	x	0	0	256fs	7.35kHz ~ 48kHz	(default)
1	x	0	1	1024fs	7.35kHz ~ 13kHz	
2	x	1	0	512fs	7.35kHz ~ 26kHz	
3	x	1	1	256fs	7.35kHz ~ 48kHz	
Others	Others			N/A	N/A	

Table 11. MCKI Frequency at EXT Slave Mode (PMPLL bit = “0”, M/S bit = “0”)
(x: Don’t care, N/A: Not Available)

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. The out-of-band noise can be improved by using higher frequency of the master clock. The S/N of the DAC output through LOUT/ROUT pins at fs=8kHz is shown in Table 12.

MCKI	S/N (fs=8kHz, 20kHzLPF + A-weighted)
256fs	83dB
512fs	95dB
1024fs	96dB

Table 12. Relationship between MCKI and S/N of LOUT/ROUT pins

The external clocks (MCKI, BICK and LRCK) must always be present whenever the ADC, DAC or Programmable Filter is in operation (PMADL bit = “1”, PMADR bit = “1”, PMDAC bit = “1” or PMPFIL bit = “1”). If these clocks are not provided, the AK4649VN may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. When the external clocks are not present, the ADC and DAC should be in the power-down mode (PMADL=PMADR=PMDAC = PMPFIL bits = “0”).

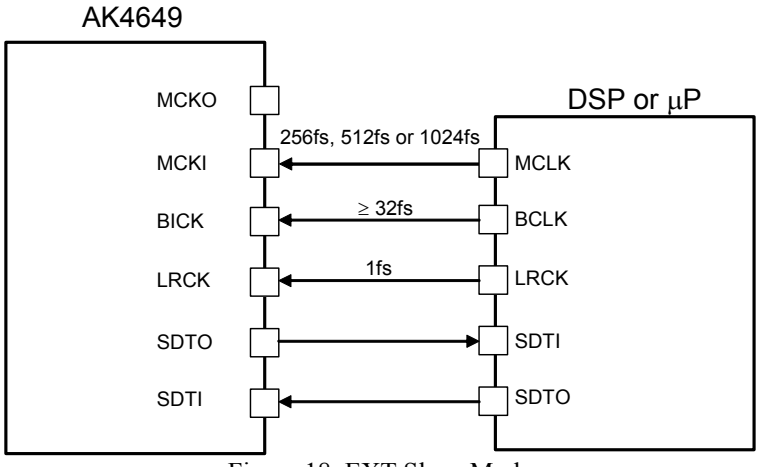


Figure 18. EXT Slave Mode

■ EXT Master Mode (PMPLL bit = "0", M/S bit = "1")

The AK4649VN becomes EXT Master Mode by setting PMPLL bit = "0" and M/S bit = "1". Master clock is input from the MCKI pin, the internal PLL circuit is not operated. The clock required to operate the AK4649VN is MCKI (256fs, 512fs or 1024fs). The input frequency of MCKI is selected by FS1-0 bits (Table 13).

Mode	FS3-2 bits	FS1 bit	FS0 bit	MCKI Input Frequency	Sampling Frequency Range	
0	x	0	0	256fs	7.35kHz ~ 48kHz	(default)
1	x	0	1	1024fs	7.35kHz ~ 13kHz	
2	x	1	0	512fs	7.35kHz ~ 26kHz	
3	x	1	1	256fs	7.35kHz ~ 48kHz	

Table 13. MCKI Frequency at EXT Master Mode (PMPLL bit = "0", M/S bit = "1") (x: Don't care)

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. The out-of-band noise can be improved by using higher frequency of the master clock. The S/N of the DAC output through LOUT/ROUT pins at fs=8kHz is shown in Table 14.

MCKI	S/N (fs=8kHz, 20kHzLPF + A-weighted)
256fs	83dB
512fs	95dB
1024fs	96dB

Table 14. Relationship between MCKI and S/N of LOUT/ROUT pins

MCKI must always be present whenever the ADC, DAC or Programmable Filter is in operation (PMADL bit = "1", PMADR bit = "1", PMDAC bit = "1" or PMPFIL bit = "1"). If MCKI is not provided, the AK4649VN may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If MCKI is not present, the ADC, DAC and Programmable Filter should be in the power-down mode (PMADL=PMADR=PMDAC= PMPFIL bits = "0").

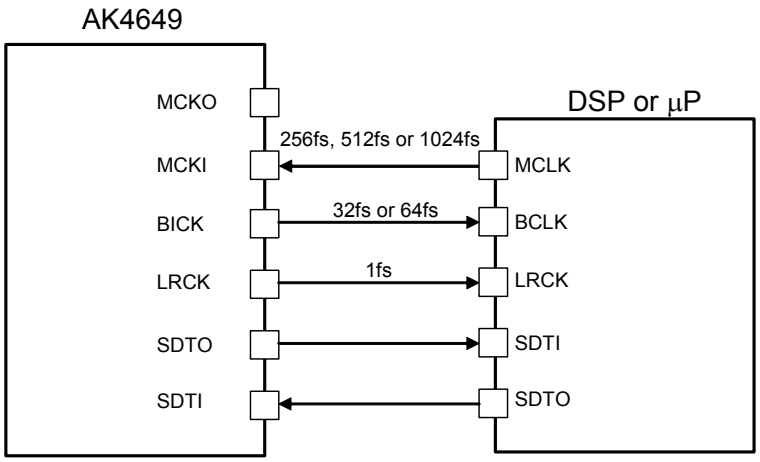


Figure 19. EXT Master Mode

BCKO bit	BICK Output Frequency	
0	32fs	(default)
1	64fs	

Table 15. BICK Output Frequency at Master Mode

■ System Reset

Upon power-up, the AK4649VN must be reset by bringing the PDN pin = "L". This ensures that all internal registers reset to their initial value. The PDN pin recommends inputting "L" at power-up.

The ADC enters an initialization cycle when the PMADL or PMADR bit is changed from "0" to "1". The initialization cycle time is set by ADRST bit (Table 16). During the initialization cycle, the ADC digital data outputs of both channels are forced to a 2's complement, "0". The ADC output reflects the analog input signal after the initialization cycle is complete. When using a digital microphone, the initialization cycle is the same as ADC's.

(Note) The initial data of ADC has offset data that depends on the condition of the microphone and the cut-off frequency of HPF. If this offset is not small, make initialization cycle longer by setting ADRST bit = "0" or do not use the initial data of ADC.

ADRST bit	Initialization Cycle			
	Cycle	fs = 8kHz	fs = 16kHz	fs = 44.1kHz
0	1059/fs	132.4ms	66.2ms	24ms
1	267/fs	33.4ms	16.7ms	6.1ms

Table 16. ADC Initialization Cycle

■ Audio Interface Format

Four types of data formats are available and selected by setting the DIF1-0 bits (Table 17). In all modes, the serial data is MSB first, 2's complement format. Audio interface formats can be used in both master and slave modes. LRCK and BICK are output from the AK4649VN in master mode, but must be input to the AK4649VN in slave mode. The SDTO is clocked out on the falling edge ("↓") of BICK and the SDTI is latched on the rising edge ("↑").

Mode	DIF1 bit	DIF0 bit	SDTO (ADC)	SDTI (DAC)	BICK	Figure	
0	0	0	24bit MSB justified	24bit LSB justified	≥ 48fs	Figure 20	
1	0	1	24bit MSB justified	16bit LSB justified	≥ 32fs	Figure 21	
2	1	0	24bit MSB justified	24bit MSB justified	≥ 48fs	Figure 22	(default)
3	1	1	I^2S Compatible	I^2S Compatible	=32fs or ≥ 48fs	Figure 23	

Table 17. Audio Interface Format

If 24-bit(16-bit) data that ADC outputs is converted to 8-bit data by removing LSB 16-bit(8-bit), "–1" at 24-bit(16-bit) data is converted to "–1" at 8-bit data. And when the DAC playbacks this 8-bit data, "–1" at 8-bit data will be converted to "–65536" at 24-bit ("–256" at 16-bit) data which is a large offset. This offset can be removed by adding the offset of "32768" at 24-bit("128" at 16-bit) to 24-bit(16-bit) data before converting to 8-bit data.

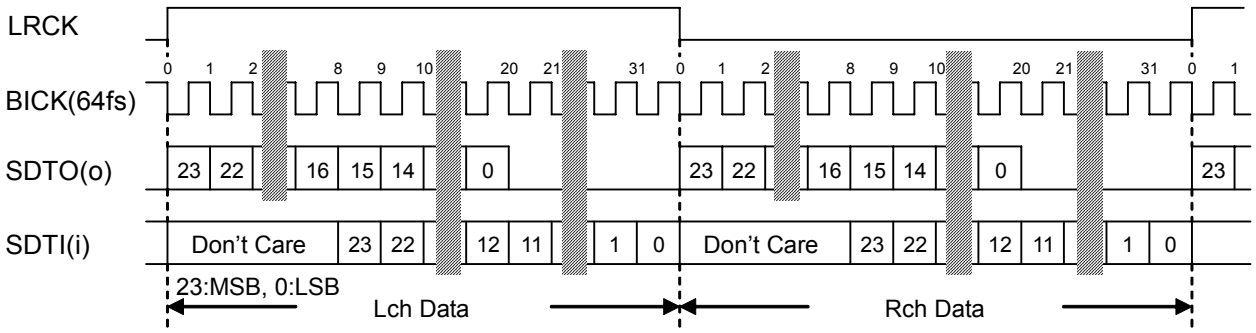


Figure 20. Mode 0 Timing

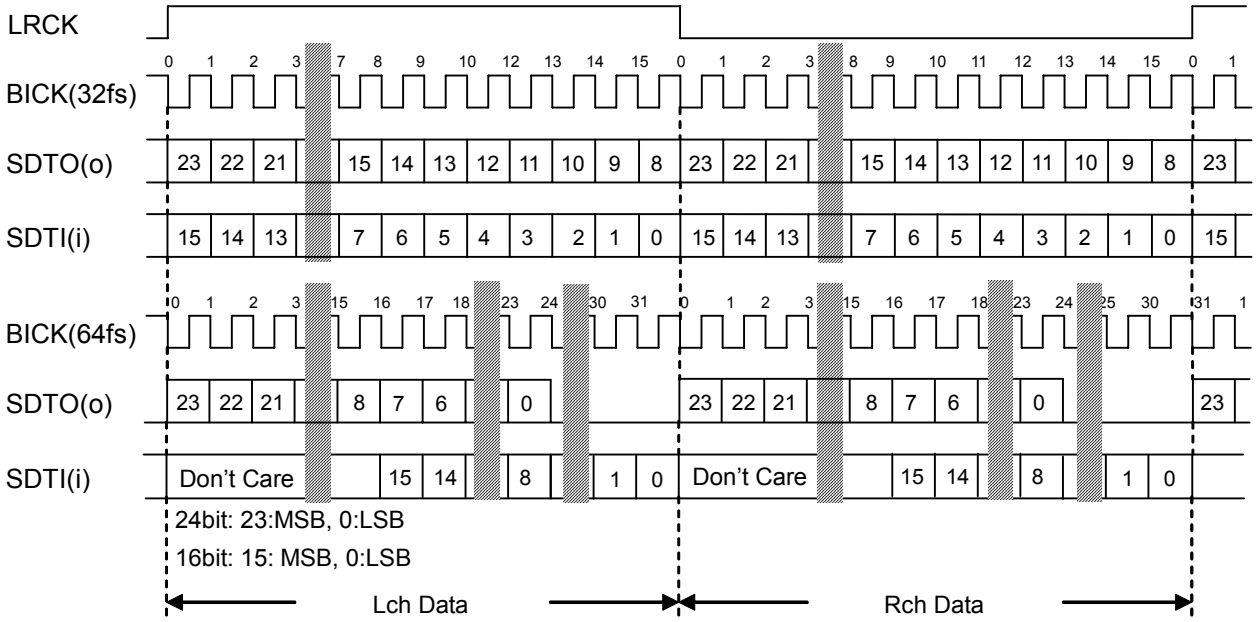


Figure 21. Mode 1 Timing

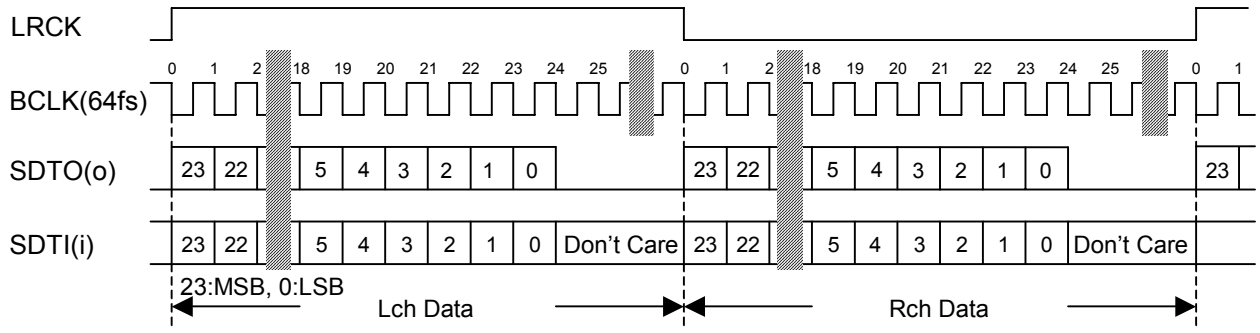


Figure 22. Mode 2 Timing

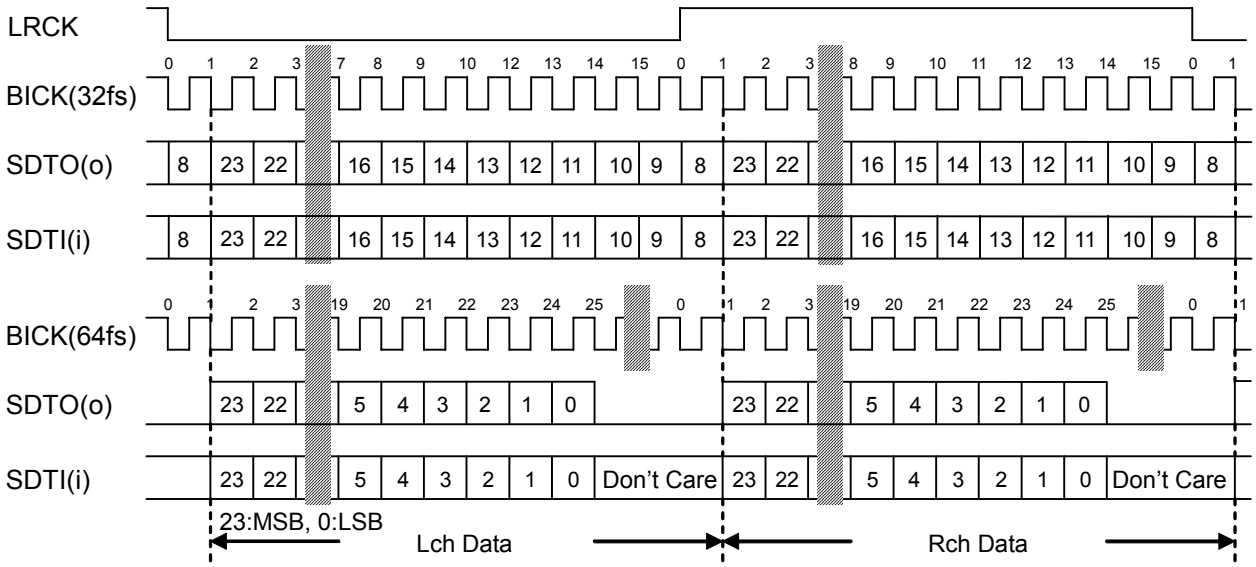


Figure 23. Mode 3 Timing

■ Mono/Stereo Mode

PMADL, PMADR, PMDML and PMDMR bits set mono/stereo ADC operation. When changing ADC operation and analog/digital microphone, PMADL, PMADR, PMDML and PMDMR bits must be set "0" at first. When PMDML or PMDMR bit is "1", PMADL and PMADR bits setting are ignored.

PMADL bit	PMADR bit	ADC Lch data	ADC Rch data	
0	0	All "0"	All "0"	(default)
0	1	Rch Input Signal	Rch Input Signal	
1	0	Lch Input Signal	Lch Input Signal	
1	1	Lch Input Signal	Rch Input Signal	

Table 18. Mono/Stereo ADC operation (Analog MIC)

PMDML bit	PMDMR bit	ADC Lch data	ADC Rch data	
0	0	All "0"	All "0"	(default)
0	1	Rch Input Signal	Rch Input Signal	
1	0	Lch Input Signal	Lch Input Signal	
1	1	Lch Input Signal	Rch Input Signal	

Table 19. Mono/Stereo ADC operation (Digital MIC)

■ MIC/LINE Input Selector

The AK4649VN has an input selector. INL and INR bits select LIN1/LIN2 and RIN1/RIN2, respectively. When DMIC bit = "1", digital microphone input is selected regardless of INL and INR bits.

DMIC bit	INL bit	INR bit	Lch	Rch	
0	0	0	LIN1	RIN1	(default)
	0	1	LIN1	RIN2	
	1	0	LIN2	RIN1	
	1	1	LIN2	RIN2	
1	0	0	Digital MIC		
	0	1			
	1	0			
	1	1			

Table 20. MIC/Line In Path Select

■ MIC Gain Amplifier

The AK4649VN has a gain amplifier for microphone input. The gain of MIC-Amp is selected by the MGAIN3-0 bits (Table 21). The typical input impedance is 30kΩ (typ).

MGAIN3 bit	MGAIN2 bit	MGAIN1 bit	MGAIN0 bit	Input Gain	
0	0	0	0	0dB	
0	0	0	1	+20dB	(default)
0	0	1	0	+26dB	
0	0	1	1	N/A	
0	1	0	0	+9dB	
0	1	0	1	+16dB	
0	1	1	0	+23dB	
0	1	1	1	+29dB	
1	0	0	0	+3dB	
1	0	0	1	+6dB	
1	0	1	0	+12dB	
Others				N/A	

Table 21. Input Gain (N/A: Not available)

■ MIC Power

When PMMP bit = "1"and MPDMP bit = "0", the MPWR pin supplies power for the microphone. This output voltage is typically 0.8 x AVDD and the load resistance is minimum 0.5kΩ. In case of using two sets of stereo microphone, the load resistance is minimum 2kΩ for each channel. Any capacitor must not be connected directly to the MPWR pin (Figure 24).

PMMP bit	MPWR pin	
0	Hi-Z	(default)
1	Output	

Table 22. MIC Power (MPDMP bit = "0")

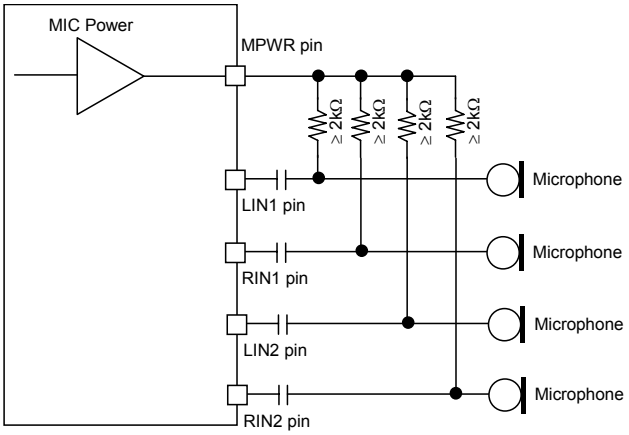


Figure 24. MIC Block Circuit

■ Digital MIC

1. Connection to Digital MIC

The AK4649VN can be connected to digital microphone by setting DMIC bit = "1". When DMIC bit is set to "1", the LIN1 and RIN1 pins become DMDAT (digital microphone data input) and DMCLK (digital microphone clock supply) pins respectively. By setting MPDMP bit = "1", the MPWR pin becomes DMP (digital microphone power supply) pin and can supply the power to the digital microphone (max. 4mA). When DMPE bit = "0", the same power supply as AVDD must be provided to the digital microphone. The Figure 25 and Figure 26 show mono/stereo connection examples. The DMCLK signal is output from the AK4649VN, and the digital microphone outputs 1bit data, which generated by ΔΣModulator, from DMDAT. PMDML/R bits control power up/down of the digital block (Decimation Filter and Digital Filter). PMADL/PMADR bits settings do not affect the digital microphone power management. The DCLKE bit controls ON/OFF of the output clock from the DMCLK pin. When the AK4649VN is powered down (PDN pin= "L"), the DMCLK and DMDAT pin are floating state. Pull-down resistors must be connected to the DMCLK and DMDAT pin externally to avoid floating state.

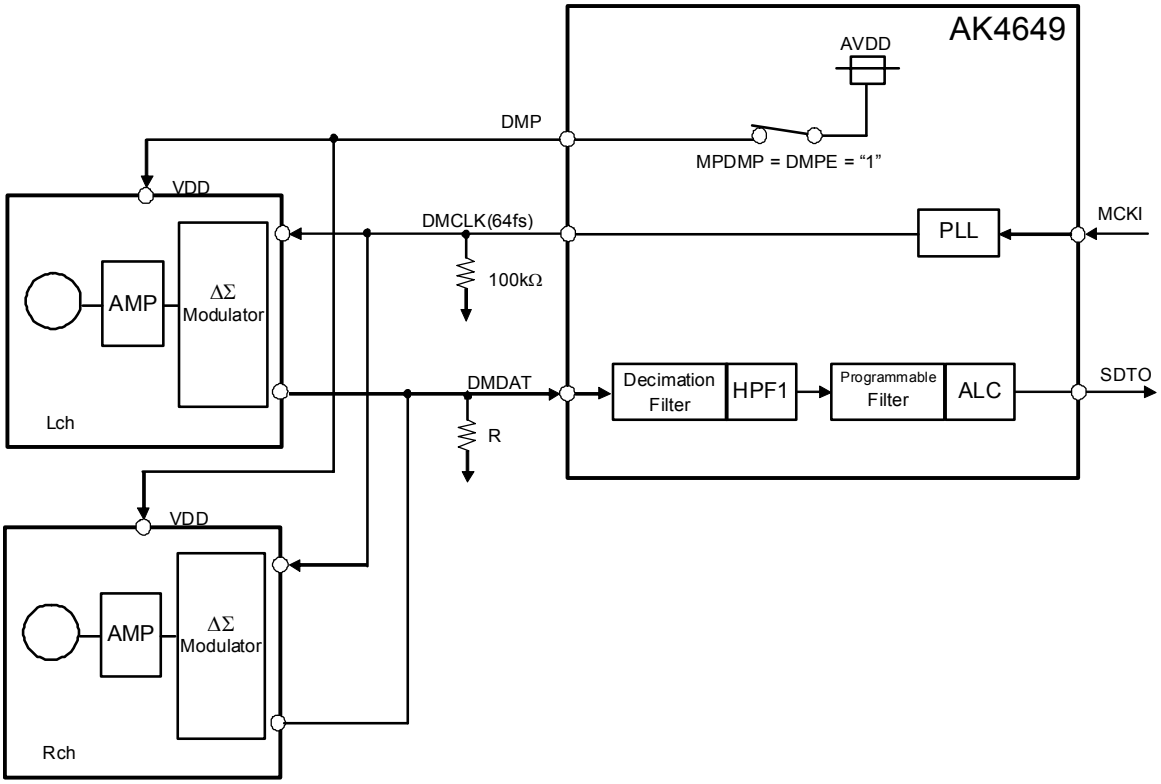


Figure 25. Connection Example of Stereo Digital MIC (MPDMP = DMPE bits = "1")

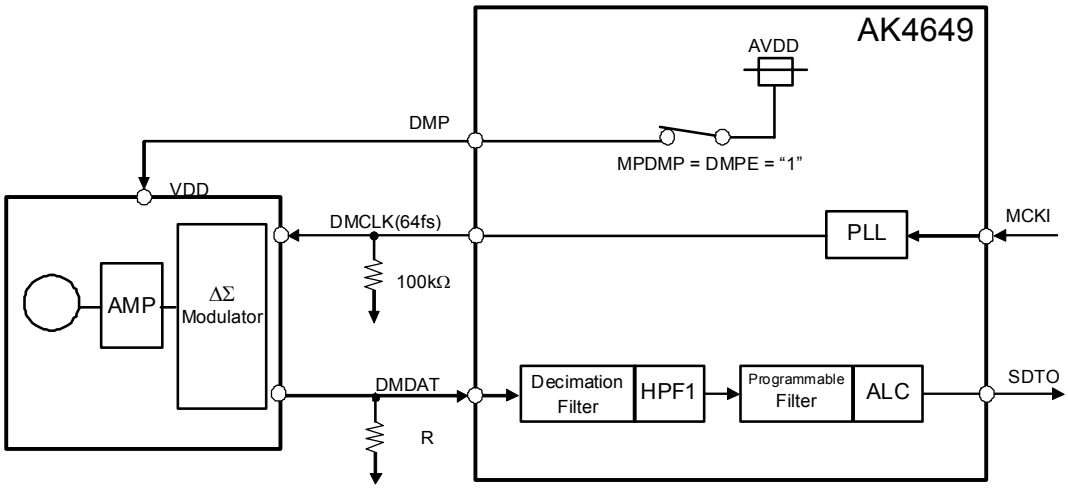


Figure 26. Connection Example of Mono Digital MIC (MPDMP = DMPE bits = "1")

2. Interface

The input data channel of the DMDAT pin is set by DCLKP bit. When DCLKP bit = "1, Lch data is input to the Decimation Filter if DMCLK = "H", Rch data is input if DMCLK = "L". When DCLKP bit = "0", Rch data is input to the Decimation Filter if DMCLK = "H", Lch data is input if DMCLK = "L". The DMCLK pin outputs "L" when DCLKE bit = "0", and only supports 64fs. In this case, necessary clocks must be supplied to the AK4649VN for ADC operation. The output data through "the Decimation and Digital Filters" is 24bit full scale when the 1bit data density is 0%~100%.

DCLKP bit	DMCLK = "H"	DMCLK = "L"	
0	Rch	Lch	(default)
1	Lch	Rch	

Figure 27. Data In/Output Timing with Digital MIC (DCLKP bit = "0")

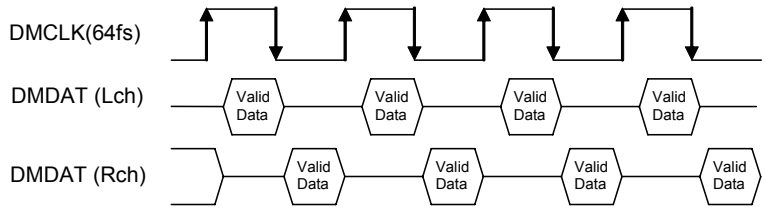


Figure 28. Data In/Output Timing with Digital MIC (DCLKP bit = "1")

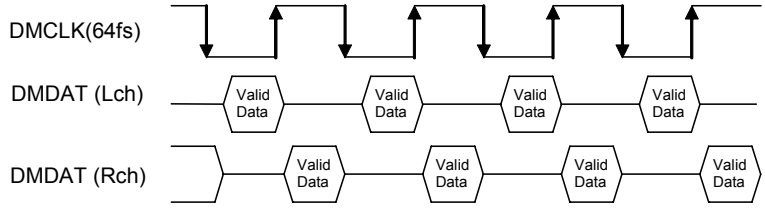
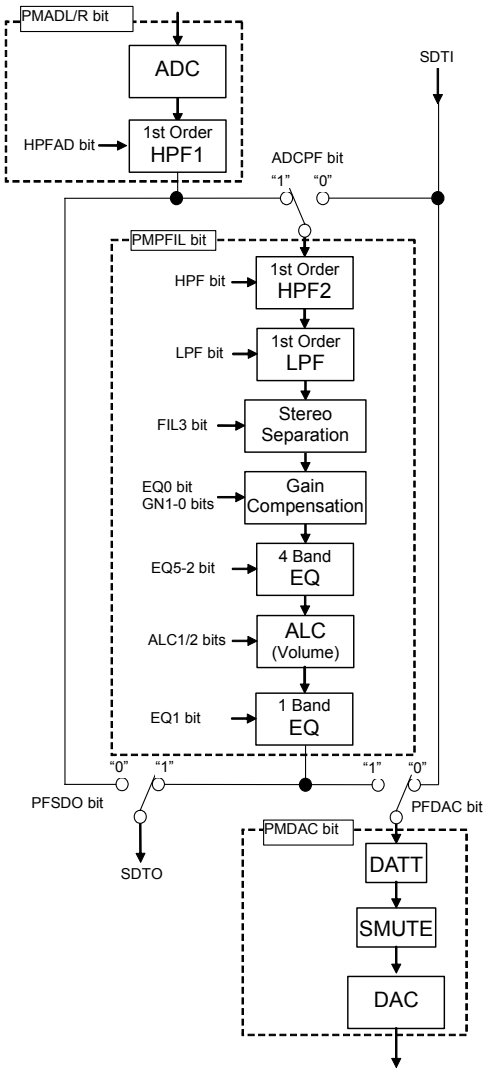


Figure 29. Data In/Output Timing with Digital MIC (DCLKP bit = "0")

■ Digital Block

The digital block consists of the blocks shown in Figure 30. Recording path and playback path is selected by setting ADCPF bit, PFDAC bit and PFSDO bit. (Figure 31 ~ Figure 34, Table 23)



(1) ADC: Include the Digital Filter (LPF) for ADC as shown in "FILTER CHRACTERISTICS".
(2) HPF1: Include the Digital Filter (HPF) for ADC as shown in "FILTER CHRACTERISTICS".
(3) DAC: Include the Digital Filter (LPF) for DAC as shown in "FILTER CHRACTERISTICS".
(4) HPF2: High Pass Filter. Applicable for use as Wind-Noise Reduction Filter. (See "Digital Programmable Filter Circuit")
(5) LPF: Low Pass Filter (See "Digital Programmable Filter Circuit")
(6) Stereo Separation: Digital Separation Emphasis Filter (See "Digital Programmable Filter Circuit")
(7) Gain Compensation: Composed of the Equalizer (EQ0) and the Gain (0dB/+12dB/+24dB). Compensate the frequency response and the gain after the Stereo Separation Emphasis Filter.
(8) 4 Band EQ: Applicable for use as Equalizer or Notch Filter. (See "Digital Programmable Filter Circuit")
(9) Volume: Input Digital Volume with ALC function. (See "Input Digital Volume" and "ALC Operation")
(10) 1 Band EQ: Applicable for use as Equalizer or Notch Filter. (See "Digital Programmable Filter Circuit")
(11) DATT: Digital volume for playback path (See "Output Digital Volume2")
(12) SMUTE: Digital volume with soft mute function (See "Output Digital Volume3")

Figure 30. Digital Block Path Select

Mode	ADCPF bit	PFDAC bit	PFSDO bit	Figure
Recording Mode 1	1	0	1	Figure 31
Playback Mode 1	0	1	0	Figure 32
Recording Mode 2 & Playback Mode 2 (Programmable Filter Bypass Mode: PMPFIL bit = "0")	x	0	0	Figure 33
Loopback Mode	1	1	1	Figure 34

Table 23. Recording Playback Mode (x: Don't care)

LPF bit, HPF bit, FIL3 bit, EQ0 bit, EQ1 bit, EQ2 bit, EQ3 bit, EQ4 bit, EQ5 bit, ACL1 bit and ALC2 bit must be "0" when changing those modes.

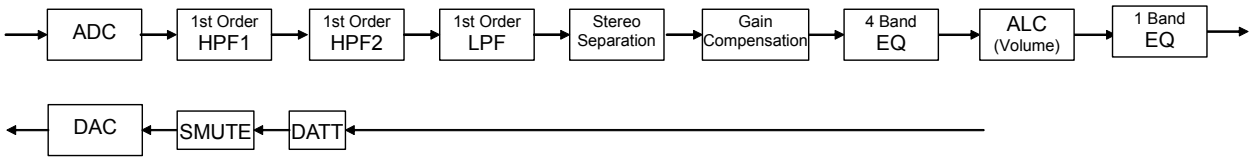


Figure 31. Path at Recording Mode 1 (default)

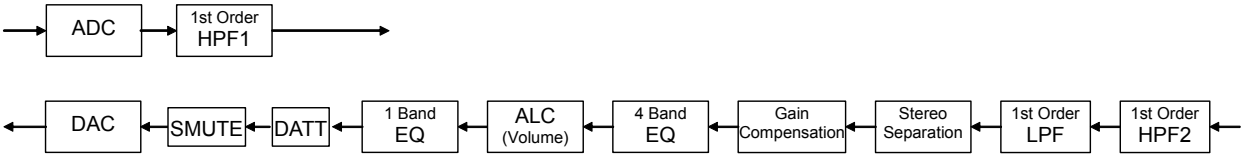


Figure 32. Path at Playback Mode 1

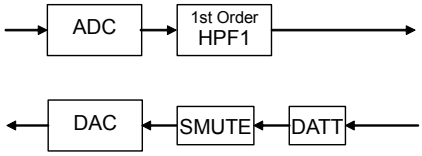


Figure 33. Path at Recording Mode 2 & Playback Mode 2

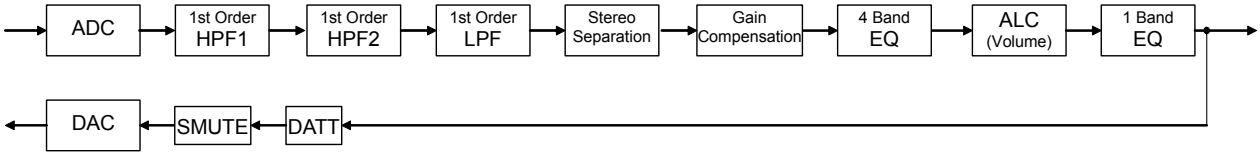


Figure 34. Path at Loopback Mode

■ Digital Programmable Filter Circuit

(1) High Pass Filter (HPF2)

Normally, this HPF is used for Wind-Noise Reduction. This is composed 1st order HPF. The coefficient of HPF is set by F1A13-0 bits and F1B13-0 bits. HPF bit controls ON/OFF of the HPF2. When the HPF2 is OFF, the audio data passes this block by 0dB gain. The coefficient must be set when HPF bit = "0" or PMPFIL bit = "0". The HPF2 starts operation 4/fs(max) after when HPF bit=PMPFIL bit= "1" is set.

fs: Sampling frequency
fc: Cut-off frequency

Register setting (Note 32)
HPF: F1A[13:0] bits =A, F1B[13:0] bits =B
(MSB=F1A13, F1B13; LSB=F1A0, F1B0)

$$A = \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency must be set as below.
fc/fs ≥ 0.0001 (fc min = 4.41Hz at 44.1kHz)

(2) Low Pass Filter (LPF)

This is composed with 1st order LPF. F2A13-0 bits and F2B13-0 bits set the coefficient of LPF. LPF bit controls ON/OFF of the LPF. When the LPF is OFF, the audio data passes this block by 0dB gain. The coefficient must be set when LPF bit = "0" or PMPFIL bit = "0". The LPF starts operation 4/fs(max) after when LPF bit =PMPFIL bit= "1" is set.

fs: Sampling frequency
fc: Cut-off frequency

Register setting (Note 32)
LPF: F2A[13:0] bits =A, F2B[13:0] bits =B
(MSB=F2A13, F1B13; LSB=F2A0, F2B0)

$$A = \frac{1}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency must be set as below.
fc/fs ≥ 0.05 (fc min = 2205Hz at 44.1kHz)

(3) Stereo Separation Emphasis Filter (FIL3)

FIL3 is used to emphasize the stereo separation of a stereo microphone recording data or playback data. F3A13-0 and F3B13-0 bits set the filter coefficient of FIL3. FIL3 becomes High Pass Filter (HPF) at F3AS bit = "0", and Low Pass Filter (LPF) at F3AS bit = "1". FIL3 bit controls ON/OFF of the FIL3. When Stereo Separation Emphasis Filter is OFF, the audio data passes this block by 0dB gain. The coefficient, must be set when FIL3 bit = "0" or PMPFIL bit = "0". The FIL3 starts operation 4/fs(max) after when FIL3 bit= PMPFIL bit= "1" is set.

1) When FIL3 is set to "HPF"

fs: Sampling frequency
fc: Cut-off frequency
K: Filter gain [dB] (0dB ≥ K ≥ −10dB)

Register setting (Note 32)
FIL3: F3AS bit = "0", F3A[13:0] bits =A, F3B[13:0] bits =B
(MSB=F3A13, F3B13; LSB=F3A0, F3B0)

$$A = 10^{K/20} \times \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

2) When FIL3 is set to "LPF"

fs: Sampling frequency
fc: Cut-off frequency
K: Filter gain [dB] (0dB ≥ K ≥ −10dB)

Register setting (Note 32)
FIL3: F3AS bit = "1", F3A[13:0] bits =A, F3B[13:0] bits =B
(MSB=F3A13, F3B13; LSB= F3A0, F3B0)

$$A = 10^{K/20} \times \frac{1}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

(4) Gain Compensation

Gain Compensation is used to compensate the frequency response and the gain that is changed by Stereo Separation Emphasis Filter. Gain Compensation is composed of the Equalizer (EQ0) and the Gain (0dB/+12dB/+24dB). E0A15-0, E0B13-0 and E0C15-0 bits set the coefficient of EQ0. GN1-0 bits set the gain (Table 24). EQ0 bit controls ON/OFF of EQ0. When EQ is OFF and the gain is 0dB, the audio data passes this block by 0dB gain. The coefficient must be set when EQ0 bit = "0" or PMPFIL bit = "0". EQ0 starts operation 4/fs(max) after when EQ0=PMPFIL bits = "1" is set.

fs: Sampling frequency
fc_1: Pole frequency
fc_2: Zero-point frequency
K: Filter gain [dB] (Maximum +12dB)

Register setting (Note 32)
E0A[15:0] bits =A, E0B[13:0] bits =B, E0C[15:0] bits =C
(MSB=E0A15, E0B13, E0C15; LSB=E0A0, E0B0, E0C0)

$$A = 10^{K/20} \times \frac{1 + 1 / \tan(\pi fc_2/fs)}{1 + 1 / \tan(\pi fc_1/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc_1/fs)}{1 + 1 / \tan(\pi fc_1/fs)}, \quad C = 10^{K/20} \times \frac{1 - 1 / \tan(\pi fc_2/fs)}{1 + 1 / \tan(\pi fc_1/fs)}$$

Transfer function

$$H(z) = \frac{A + Cz^{-1}}{1 + Bz^{-1}}$$

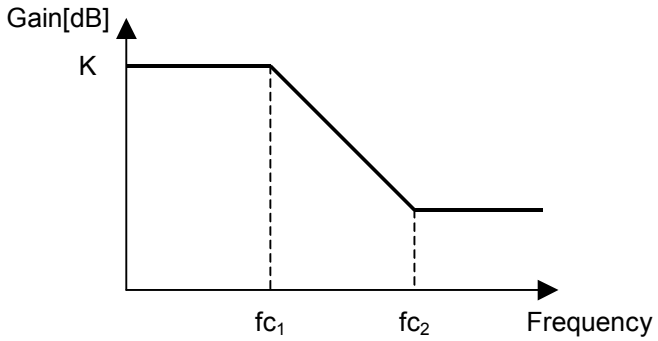


Figure 35. EQ0 Frequency Response

GN1 bit	GN0 bit	Gain	
0	0	0dB	(default)
0	1	+12dB	
1	x	+24dB	

Table 24. Gain select of gain block (x: Don't care)

(5) 4-band Equalizer & 1-band Equalizer after ALC

This block can be used as Equalizer or Notch Filter. 4-band Equalizer (EQ2, EQ3, EQ4 and EQ5) is selected ON/OFF independently by EQ2, EQ3, EQ4 and EQ5 bits. The equalizer after ALC (EQ1) is controlled by EQ1 bit. When Equalizer is OFF, the audio data passes this block by 0dB gain. E1A15-0, E1B15-0 and E1C15-0 bits set the coefficient of EQ1. E2A15-0, E2B15-0 and E2C15-0 bits set the coefficient of EQ2. E3A15-0, E3B15-0 and E3C15-0 bits set the coefficient of EQ3. E4A15-0, E4B15-0 and E4C15-0 bits set the coefficient of EQ4. E5A15-0, E5B15-0 and E5C15-0 bits set the coefficient of EQ5. The EQx (x=1~5) coefficient must be set when EQx bit = "0" or PMPFIL bit = "0". EQ1-5 start operation 4/fs(max) after when EQx (X=1~5) = PMPFIL bit = "1"is set.

fs: Sampling frequency
$fo_1 \sim fo_5$: Center frequency
$fb_1 \sim fb_5$: Band width where the gain is 3dB different from center frequency
$K_1 \sim K_5$: Gain ($-1 \le K_n \le 3$)

Register setting (Note 32)
EQ1: E1A[15:0] bits =A_1, E1B[15:0] bits =B_1, E1C[15:0] bits =C_1
EQ2: E2A[15:0] bits =A_2, E2B[15:0] bits =B_2, E2C[15:0] bits =C_2
EQ3: E3A[15:0] bits =A_3, E3B[15:0] bits =B_3, E3C[15:0] bits =C_3
EQ4: E4A[15:0] bits =A_4, E4B[15:0] bits =B_4, E4C[15:0] bits =C_4
EQ5: E5A[15:0] bits =A_5, E5B[15:0] bits =B_5, E5C[15:0] bits =C_5
(MSB=E1A15, E1B15, E1C15, E2A15, E2B15, E2C15, E3A15, E3B15, E3C15, E4A15, E4B15, E4C15, E5A15, E5B15, E5C15 ; LSB= E1A0, E1B0, E1C0, E2A0, E2B0, E2C0, E3A0, E3B0, E3C0, E4A0, E4B0, E4C0, E5A0, E5B0, E5C0)

$$A_n = K_n \times \frac{\tan(\pi fb_n/fs)}{1+\tan(\pi fb_n/fs)}, \quad B_n = \cos(2\pi\, fo_n/fs) \times \frac{2}{1+\tan(\pi fb_n/fs)}, \quad C_n = -\frac{1-\tan(\pi fb_n/fs)}{1+\tan(\pi fb_n/fs)}$$

(n = 1, 2, 3, 4, 5)

Transfer function

$$H(z) = \{1 + h_2(z) + h_3(z) + h_4(z) + h_5(z)\} \times \{1 + h_1(z)\}$$

$$h_n(z) = A_n \frac{1 - z^{-2}}{1 - B_n z^{-1} - C_n z^{-2}}$$

(n = 1, 2, 3, 4, 5)

The center frequency must be set as below.
$fo_n / fs < 0.497$

When gain of K is set to "-1", this equalizer becomes a notch filter. When EQ2 ~EQ5 is used as a notch filter, central frequency of a real notch filter deviates from the above-mentioned calculation, if its central frequency of each band is near. The control soft that is attached to the evaluation board has functions that revises a gap of frequency and calculates the coefficient. When its central frequency of each band is near, the central frequency should be revised and confirm the frequency response.

Note 32. [Translation the filter coefficient calculated by the equations above from real number to binary code (2's complement)]
X = (Real number of filter coefficient calculated by the equations above) x 2^{13}

X must be rounded to integer, and then should be translated to binary code (2's complement).
MSB of each filter coefficient setting register is sine bit.

■ ALC Operation

The ALC (Automatic Level Control) is operated by ALC block when ALC bit is "1". When ADCPF bit is "1", ALC circuit operates at recording path. When ADCPF bit is "0", ALC circuit operates at playback path. ALC1 bit controls ON/OFF of ALC operation at recording path, and ALC2 bit controls of ON/OFF of ALC operation at playback path.

Note 33. In this section, VOL means IVL and IVR for recording path, OVL and OVR for playback path.
Note 34. In this section, ALC bit means ALC1 bit for recording path, ALC2 bit for playback path.
Note 35. In this section, REF means IREF for recording path, OREF for playback path.

1. ALC Limiter Operation

During ALC limiter operation, when either Lch or Rch exceeds the ALC limiter detection level (Table 25), the VOL value (same value for both L and R) is attenuated automatically by the amount defined by the ALC limiter ATT step (Table 26). The VOL is then set to the same value for both channels.

When ZELMN bit = "0" (zero cross detection is enabled), the VOL value is changed by ALC limiter operation at the individual zero crossing points of Lch and Rch or at the zero crossing timeout. ZTM1-0 bits set the zero crossing timeout period of both ALC limiter and recovery operation (Table 27). When ALC output level exceeds full-scale at LFST bit = "1", VOL values are immediately (Period: 1/fs) changed in 1step(L/R common). When ALC output level is less than full-scale, VOL values are changed at the individual zero crossing point of each channels or at the zero crossing timeout.

When ZELMN bit = "1" (zero cross detection is disabled), VOL value is immediately (period: 1/fs) changed by ALC limiter operation. Attenuation step is fixed to 1 step regardless of the setting of LMAT1-0 bits.

The attenuate operation is executed continuously until the input signal level becomes ALC limiter detection level (Table 25) or less. After completing the attenuate operation, unless ALC bit is changed to "0", the operation repeats when the input signal level exceeds LMTH1-0 bits.

LMTH1 bit	LMTH0 bit	ALC Limiter Detection Level	ALC Recovery Waiting Counter Reset Level	
0	0	ALC Output ≥ −2.5dBFS	−2.5dBFS > ALC Output ≥ −4.1dBFS	(default)
0	1	ALC Output ≥ −4.1dBFS	−4.1dBFS > ALC Output ≥ −6.0dBFS	
1	0	ALC Output ≥ −6.0dBFS	−6.0dBFS > ALC Output ≥ −8.5dBFS	
1	1	ALC Output ≥ −8.5dBFS	−8.5dBFS > ALC Output ≥ −12dBFS	

Table 25. ALC Limiter Detection Level / Recovery Counter Reset Level

LMAT1 bit	LMAT0 bit	ALC1 Limiter ATT Step				
		ALC1 Output ≥ LMTH	ALC1 Output ≥ FS	ALC1 Output ≥ FS + 6dB	ALC1 Output ≥ FS + 12dB	
0	0	1	1	1	1	(default)
0	1	2	2	2	2	
1	0	2	4	4	8	
1	1	1	2	4	8	

Table 26. ALC Limiter ATT Step

ZTM1 bit	ZTM0 bit		Zero Crossing Timeout Period			
			8kHz	16kHz	44.1kHz	
0	0	128/fs	16ms	8ms	2.9ms	(default)
0	1	256/fs	32ms	16ms	5.8ms	
1	0	512/fs	64ms	32ms	11.6ms	
1	1	1024/fs	128ms	64ms	23.2ms	

Table 27. ALC Zero Crossing Timeout Period

2. ALC Recovery Operation

ALC recovery operation wait for the WTM2-0 bits (Table 28) to be set after completing ALC limiter operation. If the input signal does not exceed "ALC recovery waiting counter reset level" (Table 25) during the wait time, ALC recovery operation is executed. The VOL value is automatically incremented by RGAIN1-0 bits (Table 29) up to the set reference level (Table 30) with zero crossing detection which timeout period is set by ZTM1-0 bits (Table 27). Then the IVL and IVR are set to the same value for both channels. The ALC recovery operation is executed in a period set by WTM2-0 bits. If the setting of ZTM1-0 is longer than WTM2-0 and no zero crossing occurs, the ALC recovery operation is done at a period set by ZTM1-0 bits.

For example, when the current VOL value is 30H and RGAIN1-0 bits are set to "01", VOL is changed to 32H by auto limiter operation and then the input signal level is gained by 0.75dB (=0.375dB x 2). When the VOL value exceeds the reference level (REF7-0), the VOL values are not increased.

When
"ALC recovery waiting counter reset level (LMTH1-0) ≤ Output Signal < ALC limiter detection level (LMTH1-0)" during the ALC recovery operation, the waiting timer of ALC recovery operation is reset. When
"ALC recovery waiting counter reset level (LMTH1-0) > Output Signal",
the waiting timer of ALC recovery operation starts.

ALC operations correspond to the impulse noise. When the impulse noise is input, the ALC recovery operation becomes faster than a normal recovery operation. When large noise is input to a microphone instantaneously, the quality of small level in the large noise can be improved by this fast recovery operation. The speed of first recovery operation is set by RFST1-0 bits(Table 32)

WTM2 bit	WTM1 bit	WTM0 bit		ALC Recovery Operation Waiting Period			
				8kHz	16kHz	44.1kHz	
0	0	0	128/fs	16ms	8ms	2.9ms	(default)
0	0	1	256/fs	32ms	16ms	5.8ms	
0	1	0	512/fs	64ms	32ms	11.6ms	
0	1	1	1024/fs	128ms	64ms	23.2ms	
1	0	0	2048/fs	256ms	128ms	46.4ms	
1	0	1	4096/fs	512ms	256ms	92.9ms	
1	1	0	8192/fs	1024ms	512ms	185.8ms	
1	1	1	16384/fs	2048ms	1024ms	371.5ms	

Table 28. ALC Recovery Operation Waiting Period

RGAIN1 bit	RGAIN0 bit	GAIN STEP		
0	0	1 step	0.375dB	(default)
0	1	2 step	0.750dB	
1	0	3 step	1.125dB	
1	1	4 step	1.500dB	

Table 29. ALC Recovery GAIN Step

IREF7-0 bits	GAIN (dB)	Step	
F1H	+36.0	0.375dB	(default)
F0H	+35.625		
EFH	+35.25		
:	:		
E1H	+30.0		
:	:		
92H	+0.375		
91H	0.0		
90H	-0.375		
:	:		
2H	-53.625		
1H	-54.0		
0H	MUTE		

Table 30. Reference Level at ALC Recovery Operation for Recoding

OREF5-0 bits	GAIN (dB)	Step	
3CH	+36.0	1.5dB	(default)
3BH	+34.5		
3AH	+33.0		
:	:		
28H	+6.0		
:	:		
25H	+1.5		
24H	0.0		
23H	-1.5		
:	:		
2H	-51.0		
1H	-52.5		
0H	-54.0		

Table 31. Reference Level at ALC Recovery Operation for Playback

RFST1 bit	RFST0 bit	Recovery Speed	
0	0	Quad Speed	(default)
0	1	8times	
1	0	16times	
1	1	N/A	

Table 32. First Recovery Speed Setting (N/A: Not available)

3. The Volume at ALC Operation

The current volume value at ALC operation is reflected in VOL7-0 bits. It is enable to check the current volume value by reading the register value of VOL7-0 bits. (Since data reading for I^2C bus control mode is not supported, the register values are invalid when reading the VOL7-0 bits.)

VOL7-0 bits	GAIN (dB)
F1H	+36.0
F0H	+35.625
EFH	+35.25
:	:
C5H	+19.5
:	:
92H	+0.375
91H	0.0
90H	-0.375
:	:
2H	-53.625
1H	-54.0
0H	MUTE

Table 33. Value of VOL7-0 bits

4. Example of ALC Setting

Table 34 and Table 35 show the examples of the ALC setting for recording and playback path.

Register Name	Comment	fs=8kHz		fs=44.1kHz	
		Data	Operation	Data	Operation
LMTH1-0	Limiter detection Level	01	–4.1dBFS	01	–4.1dBFS
ZELMN	Limiter zero crossing detection	0	Enable	0	Enable
ZTM1-0	Zero crossing timeout period	01	32ms	11	23.2ms
WTM2-0	Recovery waiting period *WTM2-0 bits must be the same value or larger value than ZTM1-0 bits	001	32ms	100	46.4ms
IREF7-0	Maximum gain at recovery operation	E1H	+30dB	E1H	+30dB
IVL7-0, IVR7-0	Gain of IVOL	E1H	+30dB	E1H	+30dB
LMAT1-0	Limiter ATT step	00	1 step	00	1 step
LFST	Fast Limiter Operation	1	ON	1	ON
RGAIN1-0	Recovery GAIN step	00	1 step	00	1 step
RFST1-0	Fast Recovery Speed	00	4 times	00	4 times
ALC1	ALC enable	1	Enable	1	Enable

Table 34. Example of the ALC Setting (Recording)

Register Name	Comment	fs=8kHz		fs=44.1kHz	
		Data	Operation	Data	Operation
LMTH1-0	Limiter detection Level	01	–4.1dBFS	01	–4.1dBFS
ZELMN	Limiter zero crossing detection	0	Enable	0	Enable
ZTM1-0	Zero crossing timeout period	01	32ms	11	23.2ms
WTM2-0	Recovery waiting period *WTM2-0 bits must be the same value or larger value than ZTM1-0 bits	001	32ms	100	46.4ms
OREF5-0	Maximum gain at recovery operation	28H	+6dB	28H	+6dB
OVL7-0, OVR7-0	Gain of VOL	91H	0dB	91H	0dB
LMAT1-0	Limiter ATT step	00	1 step	00	1 step
LFST	Fast Limiter Operation	1	ON	1	ON
RGAIN1-0	Recovery GAIN step	00	1 step	00	1 step
RFST1-0	Fast Recovery Speed	00	4 times	00	4 times
ALC2	ALC enable	1	Enable	1	Enable

Table 35. Example of the ALC Setting (Playback)

5. Noise Suppression

The Noise Suppression is enabled when NSCE bit (Noise suppression enable bit) = "1" during ALC operation (ALC1 bit = "1"). This function attenuates output signal level automatically when minute amount of the signal is input.

NSCE bit: Noise Suppression Enable
0: Disable (default)
1: Enable

(1) Noise Level Suppressing Operation

The output signal (Note 36) is suppressed when the input peak level is lower than "Noise Suppression Threshold Low Level" set by NSTHL3-0 bits (Table 36) during the waiting time set by WTM2-0 bits (Table 28).

VOL value is changed by this noise suppressing operation only at the individual zero crossing points of Lch and Rch or at the zero crossing timeout. Noise level suppressing operation has common zero cross timeout period to ALC recovery operation which is set by ZTM1-0 bits. (Table 27)

This operation sets the volume automatically to the reference level (Table 40) with zero cross detection in the period which is set by ZTM1-0 bits (Table 27). It is executed in the cycle of WTM2-0 bits settings.

Note 36. When the input signal volume is smaller than the value set by NSREF7-0 bits, normal ALC recovery operation is executed.

NSTHL3 bit	NSTHL2 bit	NSTHL1 bit	NSTHL0 bit	Noise Suppression Threshold Low Level	
0	0	0	0	–81dB	(default)
0	0	0	1	–78dB	
0	0	1	0	–75dB	
0	0	1	1	–72dB	
0	1	0	0	–69dB	
0	1	0	1	–66dB	
0	1	1	0	–63dB	
0	1	1	1	–60dB	
1	0	0	0	–57dB	
1	0	0	1	–54dB	
1	0	1	0	–51dB	

Table 36. Noise Suppression Threshold Low Level

NATT1 bit	NATT0 bit	ATT STEP	
0	0	1/4 (Note 37)	
0	1	1/2 (Note 38)	(default)
1	0	1	
1	1	2	

Note 37. 1step attenuated in 4 x “WTM cycles”.
Note 38. 1step attenuated in 2 x “WTM cycles”.

Table 37. Noise ATT Settings

ZTM1 bit	ZTM0 bit		Zero Cross Timeout Period			
			8kHz	16kHz	44.1kHz	
0	0	128/fs	16ms	8ms	2.9ms	(default)
0	1	256/fs	32ms	16ms	5.8ms	
1	0	512/fs	64ms	32ms	11.6ms	
1	1	1024/fs	128ms	64ms	23.2ms	

Table 27. ALC Zero Cross Timeout Period Settings

(2) Noise Level Hold

During the waiting time set by WTM2-0 bits (Table 28), VOL values are kept when the input signal peak level is in between the set value of NSTHH1-0 (Note 39) and Noise Suppression Threshold Low Level (Noise Suppression High Level >input signal level ≥ Noise Suppression Threshold Low Level) therefore the output signal level does not change.

NSTHH1 bit	NSTHH0 bit	Noise Suppression High Level (Note 39)	
0	0	NSTHL3-0 bits + 3dB	
0	1	NSTHL3-0 bits + 6dB	(default)
1	0	NSTHL3-0 bits + 9dB	
1	1	NSTHL3-0 bits + 12dB	

Note 39. Noise Suppression Threshold Low Level (NSTHL3-0 bits) + Gain (NSTHH1-0 bits) = Noise Suppression High Level

Table 38. Noise Suppression High Level Settings

(3) Noise Suppression → Normal ALC Operation

During noise suppressing operation, if the input signal level exceeds Noise Suppression High Level, the operation switches to normal ALC operation from noise suppressing or noise level hold operation. In this case, recovery speed is faster than the normal recovery (Table 39).

However, when normal ALC operation is changed to noise suppressing operation and the internal volume is lower than the reference value at Noise Suppression (NSREF7-0 bits), the recovery speed is the same as the ALC recovery speed during the operation switches to normal ALC operation from noise suppressing.

NSGAIN1 bit	NSGAIN0 bit	Recovery Speed	
0	0	8 step	
0	1	12 step	(default)
1	0	16 step	
1	1	28 step	

Table 39. Fast Recovery Speed Setting from Noise Suppression to ALC Operation

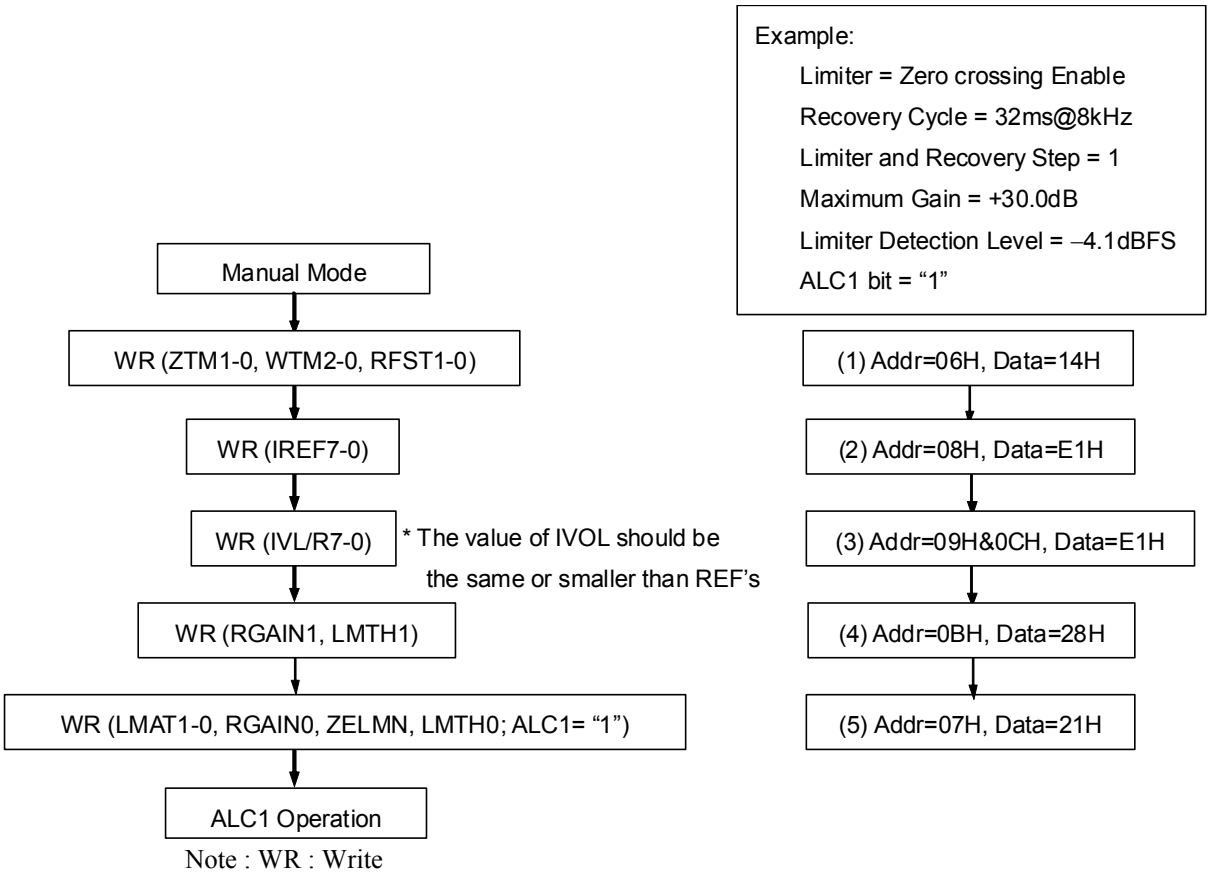
NSREF7-0 bits	GAIN[dB]	Step	
F1H	+36.0	0.375dB	
F0H	+35.625		
EFH	+35.25		
:	:		
C5H	+19.5		
:	:		
92H	+0.375		
91H	0.0		(default)
90H	–0.375		
:	:		
2H	–53.625		
1H	–54.0		
0H	MUTE		

Table 40. Reference Value Setting when Noise Suppression is ON

6. Example of registers set-up sequence of ALC1 Operation

The following registers must not be changed during ALC operation. These bits must be changed after ALC operation is finished by ALC1 bit=ALC2 bit = "0". All ALC outputs are "0" until manual mode starts when ALC1 bit =ALC2 bit = "0".

LMTH1-0, LMAT1-0, WTM2-0, ZTM1-0, RGAIN 1-0, REF7-0, ZELMN, RFST1-0, LFST, NSCE, NSTHL3-0, NATT1-0, NSTHH1-0, NSGAIN1-0, NSREF7-0



Note : WR : Write

Figure 36. Registers Set-up Sequence at ALC1 Operation (recording path)

■ Input Digital Volume (Manual Mode)

The input digital volume becomes manual mode at ALC1 bit = "0" when ADCPF bit ="1". This mode is used in the case shown below.

1. After exiting reset state, set-up the registers for ALC operation (ZTM1-0, LMTH and etc)
2. When the registers for ALC operation (Limiter period, Recovery period and etc) are changed. For example; when the change of the sampling frequency.
3. When IVOL is used as a manual volume control.

IVL7-0 and IVR7-0 bits set the gain of the volume control (Table 41). The IVOL value is changed at zero crossing or timeout. The zero crossing timeout period is set by ZTM1-0 bits. Lch and Rch volumes are set individually by IVL7-0 and IVR7-0 bits when IVOLC bit = "0". IVL7-0 bits control both Lch and Rch volumes together when IVOLC bit = "1".

IVL7-0 bits IVR7-0 bits	GAIN (dB)	Step	
F1H	+36.0	0.375dB	(default)
F0H	+35.625		
EFH	+35.25		
:	:		
E2H	+30.375		
E1H	+30.0		
E0H	+29.625		
:	:		
03H	–53.25		
02H	–53.625		
01H	–54		
00H	MUTE		

Table 41. Input Digital Volume Setting

If IVL7-0 or IVR7-0 bits are written during PMPFIL bit = "0", IVOL operation starts with the written values after PMPFIL bit is changed to "1".

When writing to IVOL7-0 bits continually, take an interval of zero crossing timeout period or more. If not, the zero crossing counter is reset at each time and the volume will not be changed. However, when writing the same register values as the previous time, the zero crossing counter will not be reset, so that it could be written in an interval less than zero crossing timeout.

■ Output Digital Volume (Manual Mode)

The ALC block becomes output digital volume (manual mode) by setting ALC2 bit to "0" when PMPFIL = PMDAC bits = "1" and ADCPF bit is "0". The output digital volume gain is set by the OVL7-0 bit and the OVR7-0 bit (Table 42). When the OVOLC bit = "1", the OVL7-0 bits control both Lch and Rch volume levels. When the OVOLC bit = "0", the OVL7-0 bits control Lch volume level and the OVR7-0 bits control Rch volume level. When changing the volumes, zero cross detect is excuted for Lch and Rch individually. The OVOL value is changed at zero crossing or timeout. The zero crossing timeout period is set by ZTM1-0 bits.

OVL7-0 bits OVR7-0 bits	GAIN (dB)	Step	
F1H	+36.0	0.375dB	
F0H	+35.625		
EFH	+35.25		
:	:		
92H	+0.375		
91H	0.0		(default)
90H	-0.375		
:	:		
2H	-53.625		
1H	-54.0		
0H	MUTE		

Table 42. Output Digital Volume Setting

When writing to the OVL7-0 bits and OVR7-0 bit continuously, the control register should be written in an interval more than zero crossing timeout. If not, the zero crossing counter is reset at each time and the volume will not be changed. H However, when writing the same register values as the previous time, the zero crossing counter will not be reset, so that it could be written in an interval less than zero crossing timeout.

■ Output Digital Volume 2

The AK4649VN has 4 steps output volume control. Lch and Rch have the same volume values, which are set by DATT1-0 bits as shown in Table 43. This volume control is also available during ALC operation.

DATT1-0 bits	GAIN (dB)	Step	
0H	0.0	6.0dB	(default)
1H	-6.0		
2H	-12.0		
3H	-18.1		

Table 43. Output Digital Volume2 Setting

■ Output Digital Volume 3

The AK4649VN has a digital output volume control (256 levels, linear step, MUTE). It is processed before the DAC block. The input data of DAC is changed from 0 to –48.13dB or MUTE. This volume has a soft transition function. Therefore no switching noise occurs during the transition. Transition time from 0dB to MUTE is 255/fs, and each 1level transition takes 1/fs. Volume calculating formula is shown in Table 45. This volume control is also available during ALC operation.

DVOL7-0 bits	ATT_DATA	GAIN(dB)	
FFH	255	+0	(default)
FEH	254	-0.034	
FDH	253	-0.068	
:	:	:	
02H	2	-42.11	
01H	1	-48.13	
00H	-	Mute	

Table 44. Output Digital Volume3 Setting

DVOL7-0 bits	GAIN (dB)
FFH : 01H	$20 \log_{10}$ (ATT_DATA / 255)
00H	Mute

Table 45. Output Digital Volume 3 Formula

■ Digital HPF1

A digital High Pass Filter (HPF) is integrated for DC offset cancellation of the ADC input. The cut-off frequencies of the HPF1 are set by HPFC1-0 bits (Table 46). It is proportional to the sampling frequency (fs) and default is 3.4Hz (@fs = 44.1kHz). HPFAD bit controls the ON/OFF of the HPF1 (Recommend HPF enable).

HPFC1 bit	HPFC0 bit	fc			
		fs=44.1kHz	fs=22.05kHz	fs=8kHz	
0	0	3.4Hz	1.7Hz	0.62Hz	(default)
0	1	13.6Hz	6.8Hz	2.47Hz	
1	0	108.8Hz	54.4Hz	19.7Hz	
1	1	217.6Hz	108.8Hz	39.5Hz	

Table 46. HPF1 Cut-off Frequency

■ De-emphasis Filter

The AK4649VN includes a digital de-emphasis filter (tc = 50/15μs) which corresponds 3 kinds frequency (32kHz, 44kHz, 48kHz) by IIR filter. Setting the DEM1-0 bits enables the de-emphasis filter (Table 47).

DEM1	DEM0	Mode	
0	0	44.1kHz	
0	1	OFF	(default)
1	0	48kHz	
1	1	32kHz	

Table 47. De-emphasis Control

■ Soft Mute

Soft mute operation is performed in the digital domain. When the SMUTE bit is set "1", the output signal is attenuated to -∞ in"ATT_DATA/fs" cycle. When the SMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to 0dB in "ATT_DATA/fs" cycle. If the soft mute is cancelled within this cycle after starting an operation, the attenuation is discontinued and it is returned to 0dB by the same cycle. Soft mute is effective for changing the signal source without stopping the signal transmission at playback path.

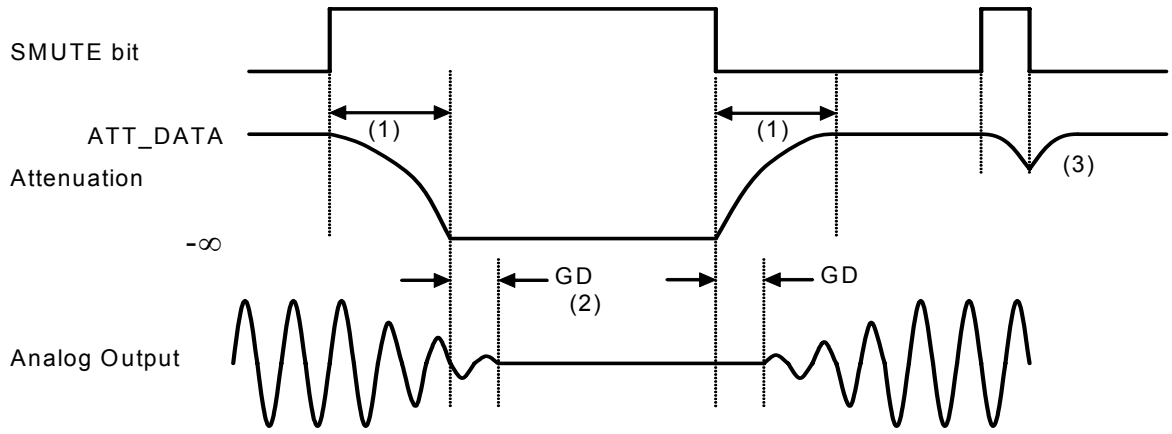


Figure 37. Soft Mute Function

(1) The input signal is attenuated by –∞ ("0") during "ATT_DATA/fs" cycle (when ATT_DATA = 0dB, 255/fs = 5.7msec@fs=44.1kHz).
(2) Analog output corresponding to digital input has group delay (GD).
(3) If soft mute is cancelled before attenuating to –∞, the attenuation is discounted and returned to ATT_DATA value within the same cycle.

■ Analog Mixing: Mono Input

When the PMBP bit is set to "1", the mono input is powered-up. When the BEEPS bit is set to "1", the input signal from the MIN pin is output to Speaker-Amp. When the BEEPH bit is set to "1", the input signal from the MIN pin is output to a stereo line output amplifier. When BPM bit is set to "0", the external resister Ri adjusts the signal level of MIN input. When BPM bit is "0", the external resister R_i is not needed. BPLVL2-0 bits control the MIN-Amp gain. Table 49, and Table 50 show the typical gain example at R_i = 33kΩ This gain is in inverse proportion to R_i

BPM bit	BEEP Mode	
0	External Resistance Mode	(default)
1	Internal Resistance Mode	

Table 48. BEEP Mode Setting

1. External Resistance Mode (BPM bit = "0")

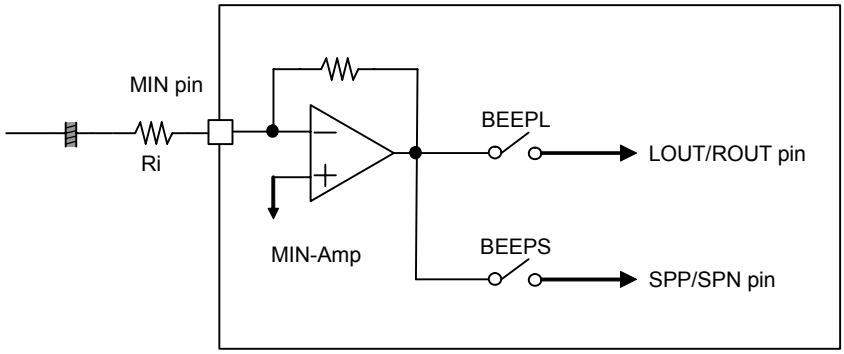


Figure 38. Block Diagram of MIN pin (BPM bit ="0")

LOVL1-0 bits	MIN → LOUT/ROUT	
00	0dB	(default)
01	+2dB	
10	+4dB	
11	+6dB	

Table 49.MIN → AOUT Output Gain (typ) at R_i = 33kΩ

SPKG1-0 bits	MIN → SPP/SPN		
	ALC2 bit = "0"	ALC2 bit = "1"	
00	+3.3dB	+5.3dB	(default)
01	+5.3dB	+7.3dB	
10	+7.3dB	+9.3dB	
11	+9.3dB	+11.3dB	

Table 50.MIN → SPK Output Gain (typ) at R_i = 33kΩ

2. Internal Resistance Mode (BPM bit = "1")

BPLVL2	BPLVL1	BPLVL0	BEEP Gain	
0	0	0	0dB	(default)
0	0	1	–3dB	
0	1	0	–6dB	
0	1	1	–12dB	
1	0	0	–18dB	
1	0	1	–23dB	
1	1	0	–29dB	
1	1	1	–34dB	

Table 51. BEEP Output Gain Setting (BPM bit = "1")

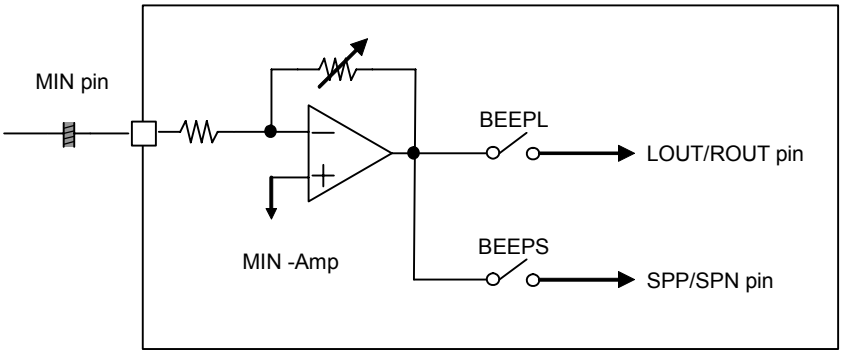


Figure 39. Block Diagram of MIN pin (BPM bit ="1")

■ Stereo Line Output (LOUT/ROUT pins)

When DACL bit is "1", Lch/Rch signal of DAC is output from the LOUT/ROUT pins which is single-ended. When DACL bit is "0", output signal is muted and LOUT/ROUT pins output VCOM voltage. The load impedance is 10kΩ (min.). When the PMLO bit = LOPS bit = "0", the stereo line output enters power-down mode and the output is pulled-down to VSS1 by 100kΩ(typ). When the LOPS bit is "1", stereo line output enters power-save mode. Pop noise at power-up/down can be reduced by changing PMLO bit when LOPS bit = "1". In this case, output signal line should be pulled-down to VSS1 by 20kΩ after AC coupled as Figure 41. Rise/Fall time is 300ms (max) at C=1μF and R_L=10kΩ. When PMLO bit = "1" and LOPS bit = "0", stereo line output is in normal operation.

LOVL bit set the gain of stereo line output.

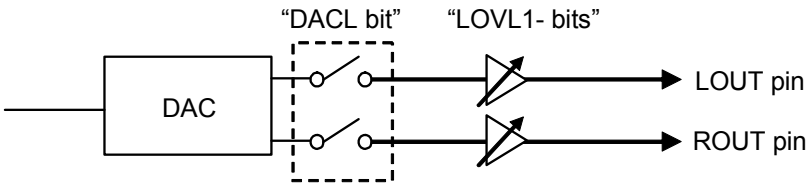


Figure 40. Stereo Line Output

LOPS	PMLO	Mode	LOUT/ROUT pin	
0	0	Power-down	Pull-down to VSS1	(default)
	1	Normal Operation	Normal Operation	
1	0	Power-save	Fall down to VSS1	
	1	Power-save	Rise up to VCOM	

Table 52. Stereo Line Output Mode Select

LOVL1-0 bits	Gain	
00	0dB	(default)
01	+2dB	
10	+4dB	
11	+6dB	

Table 53. Stereo Line Output Volume Setting

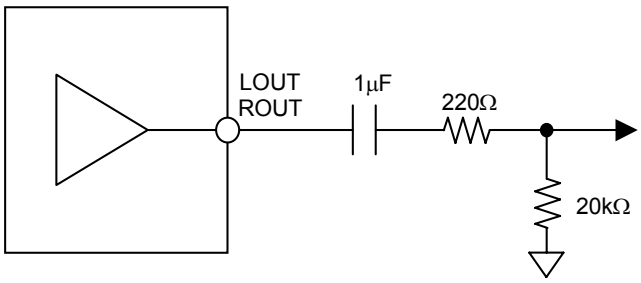


Figure 41. External Circuit for Stereo Line Output (when using Pop Noise Reduction Circuit)

[Stereo Line Output Control Sequence (when using Pop Noise Reduction Circuit)]

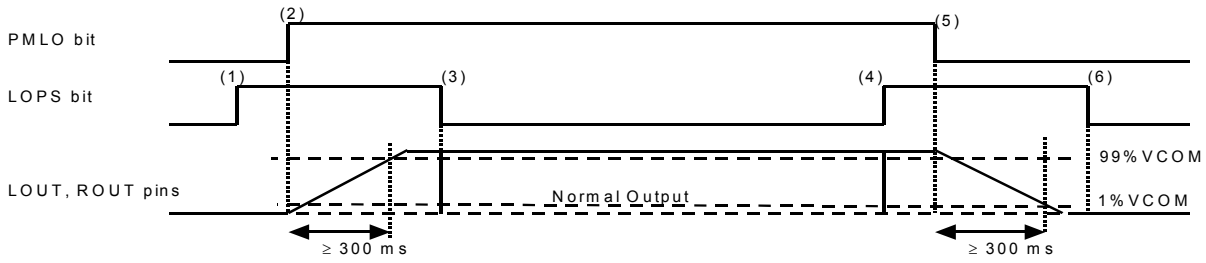


Figure 42. Stereo Line Output Control Sequence (when using Pop Noise Reduction Circuit)

(1) Set LOPS bit = "1". Stereo line output enters the power-save mode.
(2) Set PMLO bit = "1". Stereo line output exits the power-down mode.
LOUT and ROUT pins rise up to 99% VCOM voltage. Rise time is 200ms (max 300ms) at C=1μF.
(3) Set LOPS bit = "0". After LOUT and ROUT pins rise up, stereo line output exits the power-save mode.
Stereo line output is enabled.
(4) Set LOPS bit = "1". Stereo line output enters power-save mode.
(5) Set PMLO bit = "0". Stereo line output enters power-down mode.
LOUT and ROUT pins fall down to 1% VCOM voltage. Fall time is 200ms (max 300ms) at C=1μF.
(6) Set LOPS bit = "0". After LOUT and ROUT pins fall down, stereo line output exits the power-save mode

■ Speaker Output

The DAC output signal is input to the Speaker-amp as [(L+R)/2]. The Speaker-amp is mono and BTL output. The gain is set by SPKG1-0 bits. Output level depends on AVDD voltage and SPKG1-0 bits.

SPKG1-0 bits	Gain		
	ALC2 bit = "0"	ALC2 bit = "1"	
00	+3.3dB	+5.3dB	(default)
01	+5.3dB	+7.3dB	
10	+7.3dB	+9.3dB	
11	+9.3dB	+11.3dB	

Table 54. SPK-Amp Gain

SPKG1-0 bits	SPK-Amp Output (DAC Input=0dBFS, AVDD=SVDD=3.3V)	
	ALC2 bit = "0"	ALC2 bit = "1" (LMTH1-0 bits = "00")
00	3.37Vpp	3.17Vpp
01	4.23Vpp (Note 40)	4.00Vpp
10	5.33Vpp (Note 40)	5.04Vpp (Note 40)
11	6.71Vpp (Note 40)	6.33Vpp (Note 40)

Note 40. The output level is calculated by assuming that output signal is not clipped. In actual case, output signal may be clipped when DAC outputs 0dBFS signal. DAC output level should be set to lower level by setting digital volume so that Speaker-Amp output level is 4.0Vpp or less and output signal is not clipped.

Table 55. SPK-Amp Output Level

< Speaker-Amp Control Sequence >

Speaker-Amp is powered-up/down by PMSPK bit. When PMSPK bit is "0", both SPP and SPN pins are in Hi-Z state. When PMSPK bit is "1" and SPPSN bit is "0", the Speaker-Amp enters power-save mode. In this mode, the SPP pin is placed in Hi-Z state and the SPN pin outputs SVDD/2 voltage.

When the PMSPK bit is "1" after the PDN pin is changed from "L" to "H", the SPP and SPN pins rise up from power-save-mode. In this mode, the SPP pin is placed in a Hi-Z state and the SPN pin goes to SVDD/2 voltage. Because the SPP and SPN pins rise up at power-save-mode, this mode can reduce pop noise. When the AK4646 is powered-down, pop noise can be also reduced by first entering power-save-mode.

PMSPK	SPPSN	Mode	SPP	SPN	
0	x	Power-down	Hi-Z	Hi-Z	(default)
1	0	Power-save	Hi-Z	SVDD/2	
	1	Normal Operation	Normal Operation	Normal Operation	

Table 56 Speaker-Amp Mode Setting (x: Don't care)

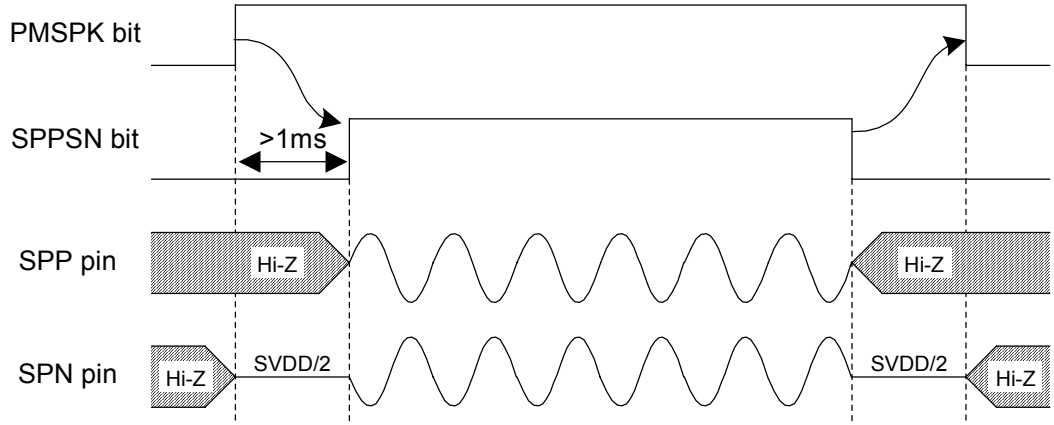


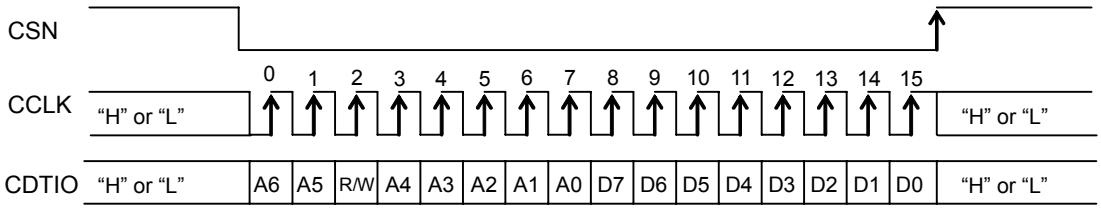
Figure 43. Power-up/Power-down Timing for Speaker-Amp

■ Serial Control Interface

(1) 3-wire Serial Control Mode

Internal registers may be written by using the 3-wire μP interface pins (CSN, CCLK and CDTIO). The data on this interface consists of Read/Write, Register address (MSB first, 7bits) and Control data (MSB first, 8bits). Each bit is clocked in on the rising edge ("↑") of CCLK. Data writing become available on the rising edge of CSN. When reading, the CDTIO pin will be output mode at the falling edge of 8th CCLIC and outputs D7-D0. The output finishes on the rising edge of CSN. The CDTIO is placed in a Hi-Z state except outputting data at read operation mode. Clock speed of CCLK is 5MHz (max). The value of internal registers are initialized by the PDN pin = "L".

Note 41. Data reading is only available on the following addresses; 00H~11H, 24H~2BH, 30~31H. When reading the address 12H ~ 23H, 2C~2FH, 32H~7FH, the register values are invalid.



R/W: READ/WRITE ("1": WRITE, "0": READ)
A6-A0: Register Address
D7-D0: Control data (Input) at Write Command
Output data (Output) at Read Command

Figure 44. Serial Control I/F Timing

(2) I2C-bus Control Mode (I2C pin = "H")

The AK4649VN supports the fast-mode I^{2}C-bus (max: 400kHz). Pull-up resistors at the SDA and SCL pins must be connected to (DVDD+0.3)V or less voltage.

(2)-1. WRITE Operations

Figure 45 shows the data transfer sequence for the I2C-bus mode. All commands are preceded by START condition. HIGH to LOW transition on the SDA line while SCL is HIGH indicates START condition (Figure 51). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant six bits of the slave address are fixed as "001001". The next bit is CAD0 (device address bit). This bit identifies the specific device on the bus. The hard-wired input pin (CAD0 pin) sets these device address bits (Figure 46). If the slave address matches that of the AK4649VN, the AK4649VN generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 52). A R/W bit value of "1" indicates that the read operation is to be executed. "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4649VN. The format is MSB first, and those most significant 2-bits are fixed to zeros (Figure 47). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 48). The AK4649VN generates an acknowledge after each byte is received. Data transfer is always terminated by STOP condition generated by the master. LOW to HIGH transition on the SDA line while SCL is HIGH defines STOP condition (Figure 51).

The AK4649VN can perform more than one byte write operation per sequence. After receipt of the third byte the AK4649VN generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 4FH prior to generating stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW (Figure 53) except for the START and STOP conditions.

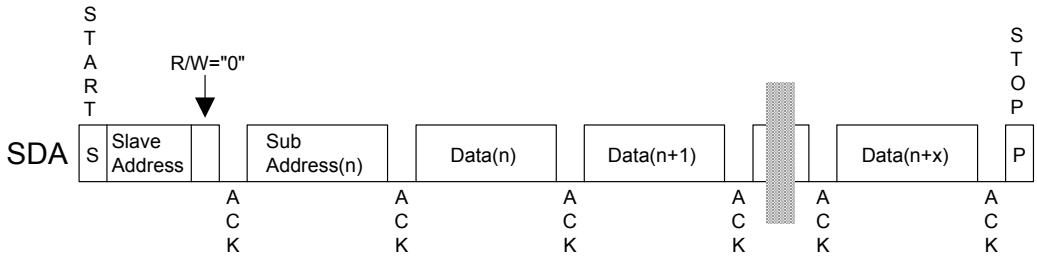


Figure 45. Data Transfer Sequence at I^{2}C Bus Mode

0	0	1	0	0	1	CAD0	R/W

Figure 46. The First Byte

0	A6	A5	A4	A3	A2	A1	A0

Figure 47. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 48. The Third Byte

(2)-2. READ Operations

Set the R/W bit = "1" for the READ operation of the AK4649VN. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 4FH prior to generating stop condition, the address counter will "roll over" to 00H and the data of 00H will be read out.

Note 42. Data reading is only available on the following addresses; 00H~0CH, 0EH ~ 11H, 24H~2BH, 30~31H. When reading the address 0DH, 12H ~ 23H, 2C~2FH, 32H~7FH, the register values are invalid.

The AK4649VN supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

(2)-2-1. CURRENT ADDRESS READ

The AK4649VN contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) were to address "n", the next CURRENT READ operation would access data from the address "n+1". After receipt of the slave address with R/W bit "1", the AK4649VN generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates stop condition instead, the AK4649VN ceases the transmission.

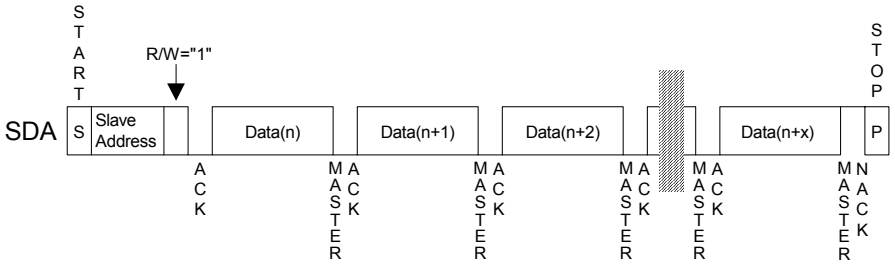


Figure 49. Current Address Read

(2)-2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit "1", the master must first perform a "dummy" write operation. The master issues a start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit "1". The AK4649VN then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4649VN ceases the transmission.

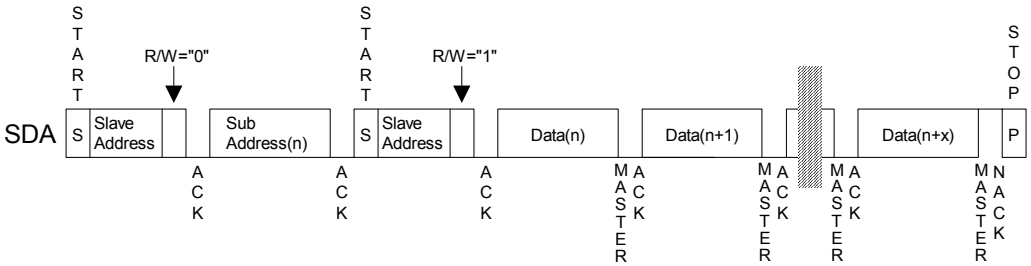


Figure 50. Random Address Read

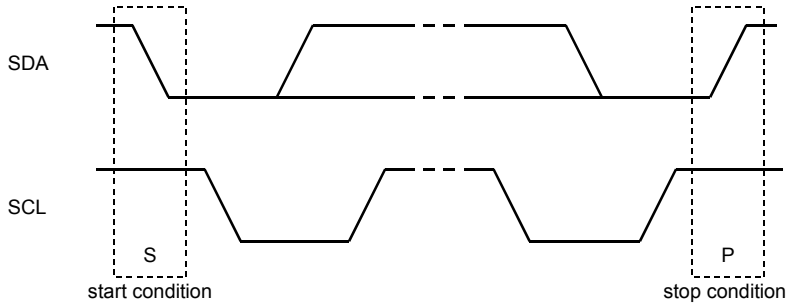


Figure 51. Start Condition and Stop Condition

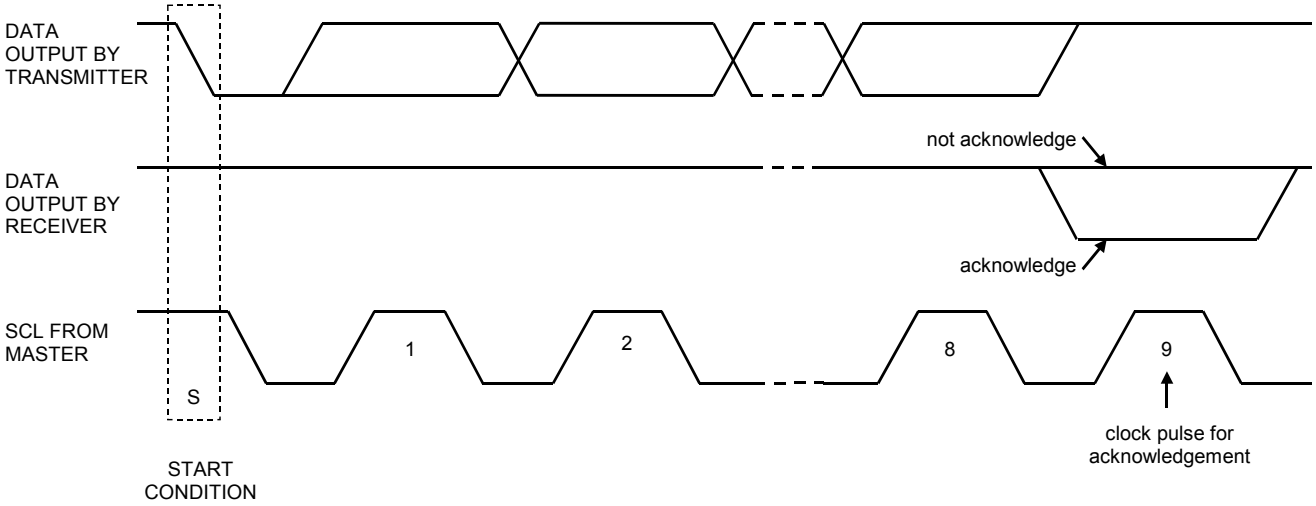


Figure 52. Acknowledge (I^2C Bus)

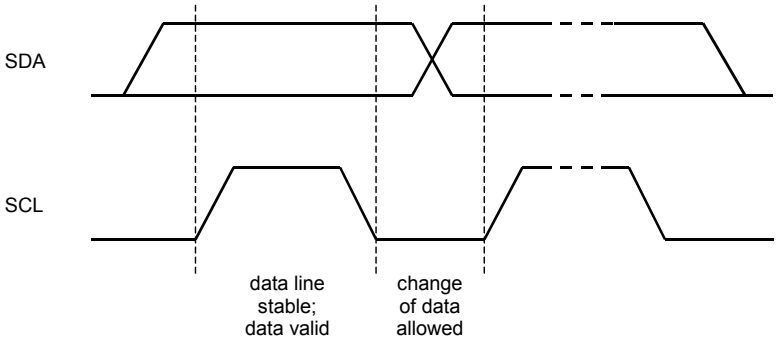


Figure 53. Bit Transfer (I^2C Bus)

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	PMPFIL	PMVCM	PMBP	PMSPK	PMLO	PMDAC	0	PMADL
01H	Power Management 2	0	0	0	0	M/S	0	MCKO	PMPLL
02H	Signal Select 1	SPPSN	BEEPS	DACS	DACL	MGAIN3	PMMP	MGAIN2	MGAIN0
03H	Signal Select 2	0	LOPS	MGAIN1	SPKG1	SPKG0	BEEPL	LOVL1	LOVL0
04H	Mode Control 1	PLL3	PLL2	PLL1	PLL0	BCKO	0	DIF1	DIF0
05H	Mode Control 2	PS1	PS0	FS3	0	0	FS2	FS1	FS0
06H	Timer Select	ADRST	WTM2	ZTM1	ZTM0	WTM1	WTM0	RFST1	RFST0
07H	ALC Mode Control 1	LFST	ALC2	ALC1	ZELMN	LMAT1	LMAT0	RGAIN0	LMTH0
08H	ALC Mode Control 2	IREF7	IREF6	IREF5	IREF4	IREF3	IREF2	IREF1	IREF0
09H	Lch Input Volume Control	IVL7	IVL6	IVL5	IVL4	IVL3	IVL2	IVL1	IVL0
0AH	Lch Output Volume Control	OVL7	OVL6	OVL5	OVL4	OVL3	OVL2	OVL1	OVL0
0BH	ALC Mode Control 3	RGAIN1	LMTH1	OREF5	OREF4	OREF3	OREF2	OREF1	OREF0
0CH	Rch Input Volume Control	IVR7	IVR6	IVR5	IVR4	IVR3	IVR2	IVR1	IVR0
0DH	ALC LEVEL	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
0EH	Mode Control 3	READ	0	SMUTE	OVOLC	DATT1	DATT0	DEM1	DEM0
0FH	Digital Volume Control	DVOL7	DVOL6	DVOL5	DVOL4	DVOL3	DVOL2	DVOL1	DVOL0
10H	Power Management 3	IVOLC	0	0	0	0	INR	INL	PMADR
11H	Digital Filter Select 1	GN1	GN0	LPF	HPF	EQ0	FIL3	0	HPFAD
12H	FIL3 Co-efficient 0	F3A7	F3A6	F3A5	F3A4	F3A3	F3A2	F3A1	F3A0
13H	FIL3 Co-efficient 1	F3AS	0	F3A13	F3A12	F3A11	F3A10	F3A9	F3A8
14H	FIL3 Co-efficient 2	F3B7	F3B6	F3B5	F3B4	F3B3	F3B2	F3B1	F3B0
15H	FIL3 Co-efficient 3	0	0	F3B13	F3B12	F3B11	F3B10	F3B9	F3B8
16H	EQ0-efficient 0	E0A7	E0A6	E0A5	E0A4	E0A3	E0A2	E0A1	E0A0
17H	EQ0-efficient 1	E0A15	E0A14	E0A13	E0A12	E0A11	E0A10	E0A9	E0A8
18H	EQ0-efficient 2	E0B7	E0B6	E0B5	E0B4	E0B3	E0B2	E0B1	E0B0
19H	EQ0-efficient 3	0	0	E0B13	E0B12	E0B11	E0B10	E0B9	E0B8
1AH	EQ0-efficient 4	E0C7	E0C6	E0C5	E0C4	E0C3	E0C2	E0C1	E0C0
1BH	EQ0-efficient 5	E0C15	E0C14	E0C13	E0C12	E0C11	E0C10	E0C9	E0C8
1CH	HPF2 Co-efficient 0	F1A7	F1A6	F1A5	F1A4	F1A3	F1A2	F1A1	F1A0
1DH	HPF2 Co-efficient 1	0	0	F1A13	F1A12	F1A11	F1A10	F1A9	F1A8
1EH	HPF2 Co-efficient 2	F1B7	F1B6	F1B5	F1B4	F1B3	F1B2	F1B1	F1B0
1FH	HPF2 Co-efficient 3	0	0	F1B13	F1B12	F1B11	F1B10	F1B9	F1B8
20H	Reserved	0	0	0	0	0	0	0	0
21H	Reserved	0	0	0	0	0	0	0	0
22H	Reserved	0	0	0	0	0	0	0	0
23H	Reserved	0	0	0	0	0	0	0	0
24H	BEEP Volume Control	0	0	0	0	0	BPLVL2	BPLVL1	BPLVL0
25H	Rch Output Volume Control	OVR7	OVR6	OVR5	OVR4	OVR3	OVR2	OVR1	OVR0
26H	Digital Filter Mode	0	0	0	0	0	PFDAC	ADCPF	PFSDO
27H	Digital MIC	0	MPDMP	PMDMR	PMDML	DCLKE	DMPE	DCLKP	DMIC
28H	BEEP/HPF Mode	HPFC1	HPFC0	0	0	0	0	0	BPM
29H	Noise Suppression 1	0	NSCE	NSTHH1	NSTHH0	NSTHL3	NSTHL2	NSTHL1	NSTHL0
2AH	Noise Suppression 2	0	0	NATT1	NATT0	0	0	NSGAIN1	NSGAIN0
2BH	Noise Suppression 3	NSREF7	NSREF6	NSREF5	NSREF4	NSREF3	NSREF2	NSREF1	NSREF 0
2CH	LPF Co-efficient 0	F2A7	F2A6	F2A5	F2A4	F2A3	F2A2	F2A1	F2A0
2DH	LPF Co-efficient 1	0	0	F2A13	F2A12	F2A11	F2A10	F2A9	F2A8
2EH	LPF Co-efficient 2	F2B7	F2B6	F2B5	F2B4	F2B3	F2B2	F2B1	F2B0
2FH	LPF Co-efficient 3	0	0	F2B13	F2B12	F2B11	F2B10	F2B9	F2B8

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
30H	Digital Filter Select 2	0	0	0	EQ5	EQ4	EQ3	EQ2	EQ1
31H	Reserved	0	0	0	0	0	0	0	0
32H	E1 Co-efficient 0	E1A7	E1A6	E1A5	E1A4	E1A3	E1A2	E1A1	E1A0
33H	E1 Co-efficient 1	E1A15	E1A14	E1A13	E1A12	E1A11	E1A10	E1A9	E1A8
34H	E1 Co-efficient 2	E1B7	E1B6	E1B5	E1B4	E1B3	E1B2	E1B1	E1B0
35H	E1 Co-efficient 3	E1B15	E1B14	E1B13	E1B12	E1B11	E1B10	E1B9	E1B8
36H	E1 Co-efficient 4	E1C7	E1C6	E1C5	E1C4	E1C3	E1C2	E1C1	E1C0
37H	E1 Co-efficient 5	E1C15	E1C14	E1C13	E1C12	E1C11	E1C10	E1C9	E1C8
38H	E2 Co-efficient 0	E2A7	E2A6	E2A5	E2A4	E2A3	E2A2	E2A1	E2A0
39H	E2 Co-efficient 1	E2A15	E2A14	E2A13	E2A12	E2A11	E2A10	E2A9	E2A8
3AH	E2 Co-efficient 2	E2B7	E2B6	E2B5	E2B4	E2B3	E2B2	E2B1	E2B0
3BH	E2 Co-efficient 3	E2B15	E2B14	E2B13	E2B12	E2B11	E2B10	E2B9	E2B8
3CH	E2 Co-efficient 4	E2C7	E2C6	E2C5	E2C4	E2C3	E2C2	E2C1	E2C0
3DH	E2 Co-efficient 5	E2C15	E2C14	E2C13	E2C12	E2C11	E2C10	E2C9	E2C8
3EH	E3 Co-efficient 0	E3A7	E3A6	E3A5	E3A4	E3A3	E3A2	E3A1	E3A0
3FH	E3 Co-efficient 1	E3A15	E3A14	E3A13	E3A12	E3A11	E3A10	E3A9	E3A8
40H	E3 Co-efficient 2	E3B7	E3B6	E3B5	E3B4	E3B3	E3B2	E3B1	E3B0
41H	E3 Co-efficient 3	E3B15	E3B14	E3B13	E3B12	E3B11	E3B10	E3B9	E3B8
42H	E3 Co-efficient 4	E3C7	E3C6	E3C5	E3C4	E3C3	E3C2	E3C1	E3C0
43H	E3 Co-efficient 5	E3C15	E3C14	E3C13	E3C12	E3C11	E3C10	E3C9	E3C8
44H	E4 Co-efficient 0	E4A7	E4A6	E4A5	E4A4	E4A3	E4A2	E4A1	E4A0
45H	E4 Co-efficient 1	E4A15	E4A14	E4A13	E4A12	E4A11	E4A10	E4A9	E4A8
46H	E4 Co-efficient 2	E4B7	E4B6	E4B5	E4B4	E4B3	E4B2	E4B1	E4B0
47H	E4 Co-efficient 3	E4B15	E4B14	E4B13	E4B12	E4B11	E4B10	E4B9	E4B8
48H	E4 Co-efficient 4	E4C7	E4C6	E4C5	E4C4	E4C3	E4C2	E4C1	E4C0
49H	E4 Co-efficient 5	E4C15	E4C14	E4C13	E4C12	E4C11	E4C10	E4C9	E4C8
4AH	E5 Co-efficient 0	E5A7	E5A6	E5A5	E5A4	E5A3	E5A2	E5A1	E5A0
4BH	E5 Co-efficient 1	E5A15	E5A14	E5A13	E5A12	E5A11	E5A10	E5A9	E5A8
4CH	E5 Co-efficient 2	E5B7	E5B6	E5B5	E5B4	E5B3	E5B2	E5B1	E5B0
4DH	E5 Co-efficient 3	E5B15	E5B14	E5B13	E5B12	E5B11	E5B10	E5B9	E5B8
4EH	E5 Co-efficient 4	E5C7	E5C6	E5C5	E5C4	E5C3	E5C2	E5C1	E5C0
4FH	E5 Co-efficient 5	E5C15	E5C14	E5C13	E5C12	E5C11	E5C10	E5C9	E5C8

Note 43. PDN pin = “L” resets the registers to their default values.
Note 44. The bits defined as 0 must contain a “0” value.
Note 45. Reading address 0DH (in I^2C-bus control mode), 12H ~ 23H, 2CH ~ 2FH and 32H ~ 7FH is not possible.
Note 46. Address 0DH is a read only register. Writing access to 0DH is ignored and does not effect the operation.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	PMPFIL	PMVCM	PMBP	PMSPK	PMLO	PMDAC	0	PMADL
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
Default		0	0	0	0	0	0	0	0

PMADL: MIC-Amp Lch and ADC Lch Power Management
0: Power-down (default)
1: Power-up
When the PMADL or PMADR bit is changed from "0" to "1", the initialization cycle (1059/fs=24ms @44.1kHz) starts. After initializing, digital data of the ADC is output.

PMDAC: DAC Power Management
0: Power-down (default)
1: Power-up

PMLO: Stereo Line Out Power Management
0: Power-down (default)
1: Power-up

PMSPK: Speaker-Amp Power Management
0: Power-down (default)
1: Power-up

PMBP: MIN Input Power Management
0: Power-down (default)
1: Power-up
Both PMDAC and PMBP bits must be set to "1" when DAC is powered-up for playback. After that, BEEPL or BEEPS bit is used to control each path when MIN input is used.

PMVCM: VCOM Power Management
0: Power-down (default)
1: Power-up

PMPFIL: Programmable Filter Block (HPF2/LPF/FIL3/EQ/5 Band EQ/ALC) Power Management
0: Power down (default)
1: Power up

All blocks can be powered-down by writing "0" to the address "00H", PMPLL, PMDML, PMDMR, DMPE, PMADR and MCKO bits. In this case, register values are maintained.

PMVCM bit must be "1" when one of bocks is powered-up. PMVCM bit can only be "0" when the address "00H" and all power management bits (PMPLL, PMMP, PMDML, PMDMR, DMPE, PMADR and MCKO) are "0".

When using either ADC, DAC or Programmable Filter (PMADL bit = "1", PMADR bit ="1", PMDAC bit = "1" or PMPFIL bit = "1"), clock must be supplied.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Power Management 2	0	0	0	0	M/S	0	MCKO	PMPLL
R/W		R	R	R	R	R/W	R	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMPLL: PLL Power Management
0: EXT Mode and Power-Down (default)
1: PLL Mode and Power-up

MCKO: Master Clock Output Enable
0: Disable: MCKO pin = "L" (default)
1: Enable: Output frequency is selected by PS1-0 bits.

M/S: Master / Slave Mode Select
0: Slave Mode (default)
1: Master Mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Signal Select 1	SPPSN	BEEPS	DACS	DACL	MGAIN3	PMMP	MGAIN2	MGAIN0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	1

MGAIN3-0: MIC-Amp Gain Control (Table 21)
MGAIN1 bit is D5 bit of 03H.

PMMP: MPWR pin Power Management
0: Power-down: Hi-Z (default)
1: Power-up

DACL: Switch Control from DAC to Stereo Line Output
0: OFF (default)
1: ON
When PMLO bit is "1", DACL bit is enabled. When PMLO bit is "0", the LOUT/ROUT pins go to VSS1.

DACS: Switch Control from DAC to Speaker-Amp
0: OFF (default)
1: ON
When DACS bit is "1", DAC output signal is input to Speaker-Amp.

BEEPS: Switch Control from MIN pin to Speaker-Amp
0: OFF (default)
1: ON
When BEEPS bit is "1", mono signal is input to Speaker-Amp.
Set BEEP input mode by BPM bit.

SPPSN: Speaker-Amp Power-Save Mode
0: Power-Save Mode (default)
1: Normal Operation
When SPPSN bit is "0", Speaker-Amp is on power-save mode. In this mode, the SPP pin goes to Hi-Z and outputs SVDD/2 voltage. When PMSPK bit = "1", SPPSN bit is enabled. After the PDN pin is set to "L", Speaker-Amp is in power-down mode since PMSPK bit is "0".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Signal Select 2	0	LOPS	MGAIN1	SPKG1	SPKG0	BEEPL	LOVL1	LOVL0
R/W		R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

LOVL1-0 : Output Stereo Line Gain Select (Table 53)
Default: 00(0dB)

BEEPL: Switch Control from MIN pin to Stereo Line Output
0: OFF (default)
1: ON
When PMLO bit is "1", BEEPL bit is enabled. When PMLO bit is "0", the LOUT/ROUT pins go to VSS1.

SPKG1-0: Speaker-Amp Output Gain Select (Table 54)

MGAIN1: MIC-Amp Gain Control (Table 21)

LOPS: Stereo Line Output Power-Save Mode
0: Normal Operation (default)
1: Power Save Mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Mode Control 1	PLL3	PLL2	PLL1	PLL0	BCKO	0	DIF1	DIF0
R/W		R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
Default		0	0	0	0	0	0	1	0

DIF1-0: Audio Interface Format (Table 17)
Default: "10" (MSB)

BCKO: BICK Output Frequency Select at Master Mode (Table 10)

PLL3-0: PLL Reference Clock Select (Note 31)
Default: "0000" (LRCK pin)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Mode Control 2	PS1	PS0	FS3	0	0	FS2	FS1	FS0
R/W		R/W	R/W	R/W	R	R	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

FS3-0: Sampling Frequency Select (Table 5, Table 6) and MCKI Frequency Select (Table 11)
FS3-0 bits select sampling frequency at PLL mode and MCKI frequency at EXT mode.

PS1-0: MCKO Output Frequency Select (Table 9)
Default: "00"(256fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Timer Select	ADRST	WTM2	ZTM1	ZTM0	WTM1	WTM0	RFST1	RFST0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

ADRST: ADC Initialization Cycle Setting
0: 1059/fs (default)
1: 267/fs

WTM2-0: ALC Recovery Waiting Period (Table 28)
A period of recovery operation when any limiter operation does not occur during ALC operation
Default is "000" (128/fs).

ZTM1-0: ALC Limiter/Recovery Operation Zero Crossing Timeout Period (Table 27)
In case of the μP WRITE operation or ALC1 recovery operation, the volume is changed at zero crossing or timeout.

RFST1-0: ALC First recovery Speed (Table 32)
Default: "00"(4times)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	ALC Mode Control 1	LFST	ALC2	ALC1	ZELMN	LMAT1	LMAT0	RGAIN0	LMTH0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

LMTH1-0: ALC Limiter Detection Level / Recovery Counter Reset Level (Table 25)
Default: "00"
LMTH1 bit is D6 bit of 0BH.

RGAIN1-0: ALC Recovery GAIN Step (Table 29)
Default: "00"
RGAIN1 bit is D7 bit of 0BH.

LMAT1-0: ALC Limiter ATT Step (Table 26)
Default: "00"

ZELMN: Zero Crossing Detection Enable at ALC Limiter Operation
0: Enable (default)
1: Disable

ALC1: ALC Enable for Recording
0: Recording ALC Disable (default)
1: Recording ALC Enable

ALC2: ALC Enable for Playback
0: Playback ALC Disable (default)
1: Playback ALC Enable

LFST: ALC Limiter operation when the output level exceed FS(Full-scale) level.
0: The volume is changed at zero crossing or zero crossing time out. (default)
1: When output of ALC is larger than FS, OVOL value is changed immediately (1/fs).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	ALC Mode Control 2	IREF7	IREF6	IREF5	IREF4	IREF3	IREF2	IREF1	IREF0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	0	0	0	0	1

IREF7-0: Reference Value at ALC Recovery Operation. 0.375dB step, 242 Level (Table 30)
Default: "E1H" (+30.0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	Lch Input Volume Control	IVL7	IVL6	IVL5	IVL4	IVL3	IVL2	IVL1	IVL0
0CH	Rch Input Volume Control	IVR7	IVR6	IVR5	IVR4	IVR3	IVR2	IVR1	IVR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	0	0	0	0	1

IVL7-0, IVR7-0: IVR7-0: Input Digital Volume; 0.375dB step, 242 Level (Table 41)
Default: "E1H" (+30.0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	Lch Output Volume Control	OVL7	OVL6	OVL5	OVL4	OVL3	OVL2	OVL1	OVL0
25H	Rch Output Volume Control	OVR7	OVR6	OVR5	OVR4	OVR3	OVR2	OVR1	OVR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	1	0	0	0	1

OVL7-0, OVR7-0: Output Digital Volume (Table 42)
Default: "91H" (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	ALC Mode Control 3	RGAIN1	LMTH1	OREF5	OREF4	OREF3	OREF2	OREF1	OREF0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	0	1	0	0	0

OREF5-0: Reference value at Playback ALC Recovery Operation. 0.375dB step, 50 Level (Table 31)
Default: "28H" (+6.0dB)

LMTH1: ALC Limiter Detection Level / Recovery Counter Reset Level (Table 25)

RGAIN1: ALC Recovery GAIN Step (Table 29)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0DH	ALC Volume	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
R/W		R	R	R	R	R	R	R	R
Default		-	-	-	-	-	-	-	-

VOL7-0: Current ALC volume value; 0.375dB step, 242 Level. Read operation only (Table 33)
Note 47. In 3-wire serial control mode. Register values are invalid when reading the address 0DH in I^2C bus control mode.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0EH	Mode Control 3	READ	0	SMUTE	OVOLC	DATT1	DATT0	DEM1	DEM0
R/W		R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	0	0	0	1

DEM1-0: De-emphasis Frequency Select (Table 47)
Default: "01" (OFF)

DATT1-0: Output Digital Volume2; 6dB step, 4 Level (Table 43)
Default: "00H" (0.0dB)

OVOLC: Output Digital Volume Control Mode Select
0: Independent
1: Dependent (default)
When OVOLC bit = "1", OVL7-0 bits control both Lch and Rch volume level, while register values of OVL7-0 bits are not written to OVR7-0 bits. When OVOLC bit = "0", OVL7-0 bits control Lch level and OVR7-0 bits control Rch level, respectively.

SMUTE: Soft Mute Control
0: Normal Operation (default)
1: DAC outputs soft-muted

READ: Read function Enable
0: Disable (default)
1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0FH	Digital Volume Control	DVOL7	DVOL6	DVOL5	DVOL4	DVOL3	DVOL2	DVOL1	DVOL0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	1	1	1	1

DVOL7-0: Output Digital Volume Control 3; Linear step (Table 43, Table 45)
Default: "FFH" (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
10H	Power Management 3	IVOLC	0	0	0	0	INR	INL	PMADR
R/W		R/W	R	R	R	R	R/W	R/W	R/W
Default		1	0	0	0	0	0	0	0

PMADR: MIC-Amp Rch, ADC Rch Power Management
0: Power down (default)
1: Power up

INL: ADC Lch Input Source Select
0: LIN1 pin (default)
1: LIN2 pin

INR: ADC Rch Input Source Select
0: RIN1 pin (default)
1: RIN2 pin

IVOLC: Input Digital Volume Control Mode Select
0: Independent
1: Dependent (default)
When IVOLC bit = "1", IVL7-0 bits control both Lch and Rch volume level, while register values of IVL7-0 bits are not written to IVR7-0 bits. When IVOLC bit = "0", IVL7-0 bits control Lch level and IVR7-0 bits control Rch level, respectively.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
11H	Digital Filter Select 1	GN1	GN0	LPF	HPF	EQ0	FIL3	0	HPFAD
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
Default		0	0	0	0	0	0	0	1

HPFAD: HPF1 Control of ADC
0: OFF
1: ON (default)
When HPFAD bit is “1”, the settings of HPFC1-0 bits are enabled. When HPFAD bit is “0”, HPFAD block is through (0dB).
When PMADL bit = “1” or PMADR bit = “1”, set HPFAD bit to “1”.

FIL3: FIL3 (Stereo Separation Emphasis Filter) Coefficient Setting Enable
0: OFF (default)
1: ON
When FIL3 bit is “1”, the settings of F3A13-0 and F3B13-0 bits are enabled.

EQ0: EQ0 (Gain Compensation Filter) Coefficient Setting Enable
0: OFF (default)
1: ON
When EQ0 bit is “1”, the settings of E0A15-0, E0B13-0 and E-C15-0 bits are enabled. When EQ0 bit is “0”, EQ block is through (0dB).

HPF: HPF2 Coefficient Setting Enable
0: OFF (default)
1: ON
When HPF bit is “1”, the settings of F1A13-0 and F1B13-0 bits are enabled. When HPF bit is “0”, HPF block is through (0dB).

LPF: LPF Coefficient Setting Enable
0: OFF (default)
1: ON
When LPF bit is “1”, the settings of F2A13-0 and F2B13-0 bits are enabled. When LPF bit is “0”, LPF block is through (0dB).

GN1-0: Gain Select at GAIN block (Table 24)
Default: “00” (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
12H	FIL3 Co-efficient 0	F3A7	F3A6	F3A5	F3A4	F3A3	F3A2	F3A1	F3A0
13H	FIL3 Co-efficient 1	F3AS	0	F3A13	F3A12	F3A11	F3A10	F3A9	F3A8
14H	FIL3 Co-efficient 2	F3B7	F3B6	F3B5	F3B4	F3B3	F3B2	F3B1	F3B0
15H	FIL3 Co-efficient 3	0	0	F3B13	F3B12	F3B11	F3B10	F3B9	F3B8
16H	EQ0-efficient 0	E0A7	E0A6	E0A5	E0A4	E0A3	E0A2	E0A1	E0A0
17H	EQ0-efficient 1	E0A15	E0A14	E0A13	E0A12	E0A11	E0A10	E0A9	E0A8
18H	EQ0-efficient 2	E0B7	E0B6	E0B5	E0B4	E0B3	E0B2	E0B1	E0B0
19H	EQ0-efficient 3	0	0	E0B13	E0B12	E0B11	E0B10	E0B9	E0B8
1AH	EQ0-efficient 4	E0C7	E0C6	E0C5	E0C4	E0C3	E0C2	E0C1	E0C0
1BH	EQ0-efficient 5	E0C15	E0C14	E0C13	E0C12	E0C11	E0C10	E0C9	E0C8
R/W		W	W	W	W	W	W	W	W
Default		0	0	0	0	0	0	0	0

F3A13-0, F3B13-0: FIL3 (Stereo Separation Emphasis Filter) Coefficient (14bit x 2)
Default: “0000H”

F3AS: FIL3 (Stereo Separation Emphasis Filter) Select
0: HPF (default)
1: LPF

E0A15-0, E0B13-0, E0C15-C0: EQ (Gain Compensation Filter) Coefficient (16bit x 2 + 14bit x 1)
Default: “0000H”

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1CH	HPF Co-efficient 0	F1A7	F1A6	F1A5	F1A4	F1A3	F1A2	F1A1	F1A0
1DH	HPF Co-efficient 1	0	0	F1A13	F1A12	F1A11	F1A10	F1A9	F1A8
1EH	HPF Co-efficient 2	F1B7	F1B6	F1B5	F1B4	F1B3	F1B2	F1B1	F1B0
1FH	HPF Co-efficient 3	0	0	F1B13	F1B12	F1B11	F1B10	F1B9	F1B8
R/W		W	W	W	W	W	W	W	W
Default		F1A13-0 bits = 0x1FA9, F1B13-0 bits = 0x20AD							

F1A13-0, F1B13-0: HPF2 Coefficient (14bit x 2)
Default: F1A13-0 bits = 0x1FA9, F1B13-0 bits = 0x20AD
fc = 150Hz@fs=44.1kHz

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
24H	BEEP Volume Control	0	0	0	0	0	BPLVL2	BPLVL1	BPLVL0
R/W		R	R	R	R	R	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

BPLVL2-0 : BEEP Sound Output Level (Table 51)
Default: “0H”: 0dB

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
26H	Digital Filter Mode	0	0	0	0	0	PFDAC	ADCPF	PFSDO
R/W		R	R	R	R	R	R/W	R/W	R/W
Default		0	0	0	0	0	0	1	1

PFSDO: SDTO Output Signal Select
0: ADC (+ 1st HPF) Output
1: Programmable Filter / ALC Output (default)

ADCPF: Programmable Filter / ALC Input Signal Select
0: SDTI
1: ADC Output (default)

PFDAC: DAC Input Signal Select
0: SDTI (default)
1: Programmable Filter / ALC Output

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
27H	Digital MIC	0	MPDMP	PMDMR	PMDML	DCLKE	DMPE	DCLKP	DMIC
R/W		R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DMIC: Digital Microphone Connection Select
0: Analog Microphone (default)
1: Digital Microphone

DCLKP: Data Latching Edge Select
0: Lch data is latched on the DMCLK rising edge (“↑”). (default)
1: Lch data is latched on the DMCLK falling edge (“↓”).

DMPE: Digital Microphone Power Supply
0: Externally (the same supply as AVDD) (default)
1: DMP pin

DCLKE: DMCLK pin Output Clock Control
0: “L” Output (default)
1: 64fs Output

PMDML/R: Input Signal Select with Digital Microphone (Table 20)
Default: “00”
ADC digital block is powered-down by PMDML = PMDMR bits = “0” when selecting a digital microphone input (DMIC bit = “1”, INL/R bits = “00”, “01” or “10”).

MPDMP: Analog / Digital Microphone Power Supply Pin Select
0: Power Supply for Analog Microphone: MPWR pin (default)
1: Power Supply for Digital Microphone: DMP pin

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
28H	BEEP/HPF Mode	HPFC1	HPFC0	0	0	0	0	0	BPM
R/W		R/W	R\/W	R	R	R	R	R	R/W
Default		0	0	0	0	0	0	0	0

BPM: BEEP Mode Setting (Table 48)
Default: “0”: External Resistance Mode

HPFC1-0: Cut-off Frequency Setting of HPF1 (ADC) (Table 46)
Default: “00” (3.4Hz @ fs = 44.1kHz)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
29H	Noise Suppression 1	0	NSCE	NSTHH1	NSTHH0	NSTHL3	NSTHL2	NSTHL1	NSTHL0
R/W		R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	0	0	0	0

NSTHL3-0: Noise Suppression Threshold Low Level Setting (Table 36)
Default: “0000” (-81dBFS)

NSTHH1-0: Noise Suppression Threshold High Level Setting (Table 38)
Default: “01” (NSTHL3-0 bits + 6dB)

NSCE: Noise Suppression Enable
0: Disable (default)
1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2AH	Noise Suppression 2	0	0	NATT1	NATT0	0	0	NSGAIN1	NSGAIN0
R/W		R	R	R/W	R/W	R	R	R/W	R/W
Default		0	0	0	1	0	0	0	1

NSGAIN1-0: ALC First Recovery Speed Setting after Noise Suppression (Table 39)
Default: “01” (8 step)

NATT1-0: Noise Attenuate Step Setting (Table 37)
Default: “01” (1/2 step)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2BH	Noise Suppression 3	NSREF7	NSREF6	NSREF5	NSREF4	NSREF3	NSREF2	NSREF1	NSREF0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	1	0	0	0	1

NSREF7-0: Reference Level Setting at Noise Suppression
0.375dB step, 242 Level (Table 40)
Default: “91H” (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2CH	LPF Co-efficient 0	F2A7	F2A6	F2A5	F2A4	F2A3	F2A2	F2A1	F2A0
2DH	LPF Co-efficient 1	0	0	F2A13	F2A12	F2A11	F2A10	F2A9	F2A8
2EH	LPF Co-efficient 2	F2B7	F2B6	F2B5	F2B4	F2B3	F2B2	F2B1	F2B0
2FH	LPF Co-efficient 3	0	0	F2B13	F2B12	F2B11	F2B10	F2B9	F2B8
R/W		W	W	W	W	W	W	W	W
Default		0	0	0	0	0	0	0	0

F2A13-0, F2B13-0: LPF Coefficient (14bit x 2)
Default: "0000H"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
30H	Digital Filter Select 2	0	0	0	EQ5	EQ4	EQ3	EQ2	EQ1
R/W		R	R	R	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

EQ1: Equalizer 1 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ1 bit is "1", the settings of E1A15-0, E1B15-0 and E1C15-0 bits are enabled. When EQ1 bit is "0", EQ1 block is through (0dB).

EQ2: Equalizer 2 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ2 bit is "1", the settings of E2A15-0, E2B15-0 and E2C15-0 bits are enabled. When EQ2 bit is "0", EQ2 block is through (0dB).

EQ3: Equalizer 3 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ3 bit is "1", the settings of E3A15-0, E3B15-0 and E3C15-0 bits are enabled. When EQ3 bit is "0", EQ3 block is through (0dB).

EQ4: Equalizer 4 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ4 bit is "1", the settings of E4A15-0, E4B15-0 and E4C15-0 bits are enabled. When EQ4 bit is "0", EQ4 block is through (0dB).

EQ5: Equalizer 5 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ5 bit is "1", the settings of E5A15-0, E5B15-0 and E5C15-0 bits are enabled. When EQ5 bit is "0", EQ5 block is through (0dB).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
32H	E1 Co-efficient 0	E1A7	E1A6	E1A5	E1A4	E1A3	E1A2	E1A1	E1A0
33H	E1 Co-efficient 1	E1A15	E1A14	E1A13	E1A12	E1A11	E1A10	E1A9	E1A8
34H	E1 Co-efficient 2	E1B7	E1B6	E1B5	E1B4	E1B3	E1B2	E1B1	E1B0
35H	E1 Co-efficient 3	E1B15	E1B14	E1B13	E1B12	E1B11	E1B10	E1B9	E1B8
36H	E1 Co-efficient 4	E1C7	E1C6	E1C5	E1C4	E1C3	E1C2	E1C1	E1C0
37H	E1 Co-efficient 5	E1C15	E1C14	E1C13	E1C12	E1C11	E1C10	E1C9	E1C8
38H	E2 Co-efficient 0	E2A7	E2A6	E2A5	E2A4	E2A3	E2A2	E2A1	E2A0
39H	E2 Co-efficient 1	E2A15	E2A14	E2A13	E2A12	E2A11	E2A10	E2A9	E2A8
3AH	E2 Co-efficient 2	E2B7	E2B6	E2B5	E2B4	E2B3	E2B2	E2B1	E2B0
3BH	E2 Co-efficient 3	E2B15	E2B14	E2B13	E2B12	E2B11	E2B10	E2B9	E2B8
3CH	E2 Co-efficient 4	E2C7	E2C6	E2C5	E2C4	E2C3	E2C2	E2C1	E2C0
3DH	E2 Co-efficient 5	E2C15	E2C14	E2C13	E2C12	E2C11	E2C10	E2C9	E2C8
3EH	E3 Co-efficient 0	E3A7	E3A6	E3A5	E3A4	E3A3	E3A2	E3A1	E3A0
3FH	E3 Co-efficient 1	E3A15	E3A14	E3A13	E3A12	E3A11	E3A10	E3A9	E3A8
40H	E3 Co-efficient 2	E3B7	E3B6	E3B5	E3B4	E3B3	E3B2	E3B1	E3B0
41H	E3 Co-efficient 3	E3B15	E3B14	E3B13	E3B12	E3B11	E3B10	E3B9	E3B8
42H	E3 Co-efficient 4	E3C7	E3C6	E3C5	E3C4	E3C3	E3C2	E3C1	E3C0
43H	E3 Co-efficient 5	E3C15	E3C14	E3C13	E3C12	E3C11	E3C10	E3C9	E3C8
44H	E4 Co-efficient 0	E4A7	E4A6	E4A5	E4A4	E4A3	E4A2	E4A1	E4A0
45H	E4 Co-efficient 1	E4A15	E4A14	E4A13	E4A12	E4A11	E4A10	E4A9	E4A8
46H	E4 Co-efficient 2	E4B7	E4B6	E4B5	E4B4	E4B3	E4B2	E4B1	E4B0
47H	E4 Co-efficient 3	E4B15	E4B14	E4B13	E4B12	E4B11	E4B10	E4B9	E4B8
48H	E4 Co-efficient 4	E4C7	E4C6	E4C5	E4C4	E4C3	E4C2	E4C1	E4C0
49H	E4 Co-efficient 5	E4C15	E4C14	E4C13	E4C12	E4C11	E4C10	E4C9	E4C8
4AH	E5 Co-efficient 0	E5A7	E5A6	E5A5	E5A4	E5A3	E5A2	E5A1	E5A0
4BH	E5 Co-efficient 1	E5A15	E5A14	E5A13	E5A12	E5A11	E5A10	E5A9	E5A8
4CH	E5 Co-efficient 2	E5B7	E5B6	E5B5	E5B4	E5B3	E5B2	E5B1	E5B0
4DH	E5 Co-efficient 3	E5B15	E5B14	E5B13	E5B12	E5B11	E5B10	E5B9	E5B8
4EH	E5 Co-efficient 4	E5C7	E5C6	E5C5	E5C4	E5C3	E5C2	E5C1	E5C0
4FH	E5 Co-efficient 5	E5C15	E5C14	E5C13	E5C12	E5C11	E5C10	E5C9	E5C8
R/W		W	W	W	W	W	W	W	W
Default		0	0	0	0	0	0	0	0

E1A15-0, E1B15-0, E1C15-0: Equalizer 1 Coefficient (16bit x3)
Default: “0000H”

E2A15-0, E2B15-0, E2C15-0: Equalizer 2 Coefficient (16bit x3)
Default: “0000H”

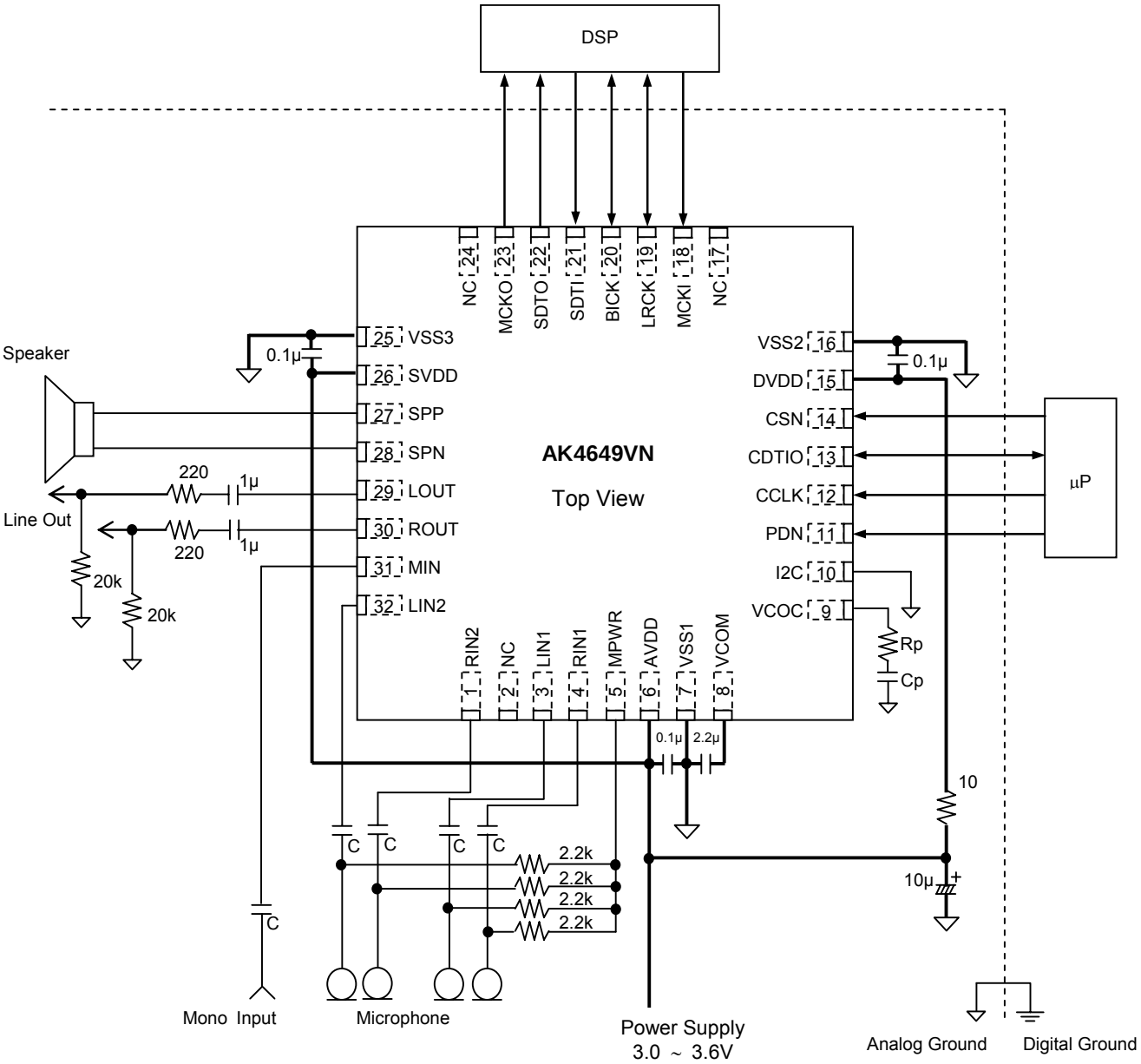
E3A15-0, E3B15-0, E3C15-0: Equalizer 3 Coefficient (16bit x3)
Default: “0000H”

E4A15-0, E4B15-0, E4C15-0: Equalizer 4 Coefficient (16bit x3)
Default: “0000H”

E5A15-0, E5B15-0, E5C15-0: Equalizer 5 Coefficient (16bit x3)
Default: “0000H”

SYSTEM DESIGN

Figure 54 shows the system connection diagram. An evaluation board (AKD4649) is available for fast evaluation as well as suggestions for peripheral circuitry.



Notes:

- VSS1, VSS2 and VSS3 of the AK4649VN must be distributed separately from the ground of external controllers.
- All digital input pins must not be left floating.
- When the AK4649VN is EXT mode (PMPLL bit = "0"), a resistor and capacitor of VCOC pin is not needed.
- When the AK4649VN is PLL mode (PMPLL bit = "1"), a resistor and capacitor of VCOC pin is shown in Table 4.
- When the AK4649VN is used at master mode, LRCK and BICK pins are floating before M/S bit is changed to "1". Therefore, around 100kΩ pull-up resistor must be connected to LRCK and BICK pins of the AK4649VN.

Figure 54. System Connection Diagram (3-wire Serial Mode, Internal Resistance Mode; BPM bit = "1")

1. Grounding and Power Supply Decoupling

The AK4649VN requires careful attention to power supply and grounding arrangements. AVDD, DVDD and SVDD are usually supplied from the system's analog supply. If AVDD, DVDD and SVDD are supplied separately, the power-up sequence is not critical. VSS1, VSS2 and VSS3 of the AK4649VN must be connected to the analog ground plane. System analog ground and digital ground must be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors must be as near to the AK4649VN as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference

VCOM is a signal ground of this chip. A 2.2μF electrolytic capacitor in parallel with a 0.1μF ceramic capacitor must be attached to the VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from the VCOM pin. All signals, especially clocks, must be kept away from the VCOM pin in order to avoid unwanted coupling into the AK4649VN.

3. Analog Inputs

The MIC and Line inputs are single-ended. The inputs signal range scales with nominally at typ. 0.07 x AVDD Vpp (@ MGAIN = +20dB) and typ. 0.7 x AVDD Vpp (@ MGAIN = 0dB), centered around the internal common voltage (typ. 0.5 x AVDD). Usually the input signal is AC coupled using a capacitor. The cut-off frequency is $fc = 1/(2\pi RC)$. The AK4649VN can accept input voltages from VSS1 to AVDD.

4. Analog Outputs

The input data format for the DAC is 2's complement. The output voltage is a positive full scale for 7FFFFFH (@24bit) and a negative full scale for 800000H (@24bit). The ideal output is VCOM voltage for 000000H (@24bit). Stereo Line Output is centered at typ. 0.5 x AVDD. The Headphone-Amp and Speaker-Amp outputs are centered at typ. 0.5 x SVDD.

CONTROL SEQUENCE

■ Clock Set up

When ADC, DAC, Digital MIC or Programmable Filter is powered-up, the clocks must be supplied.

1. PLL Master Mode

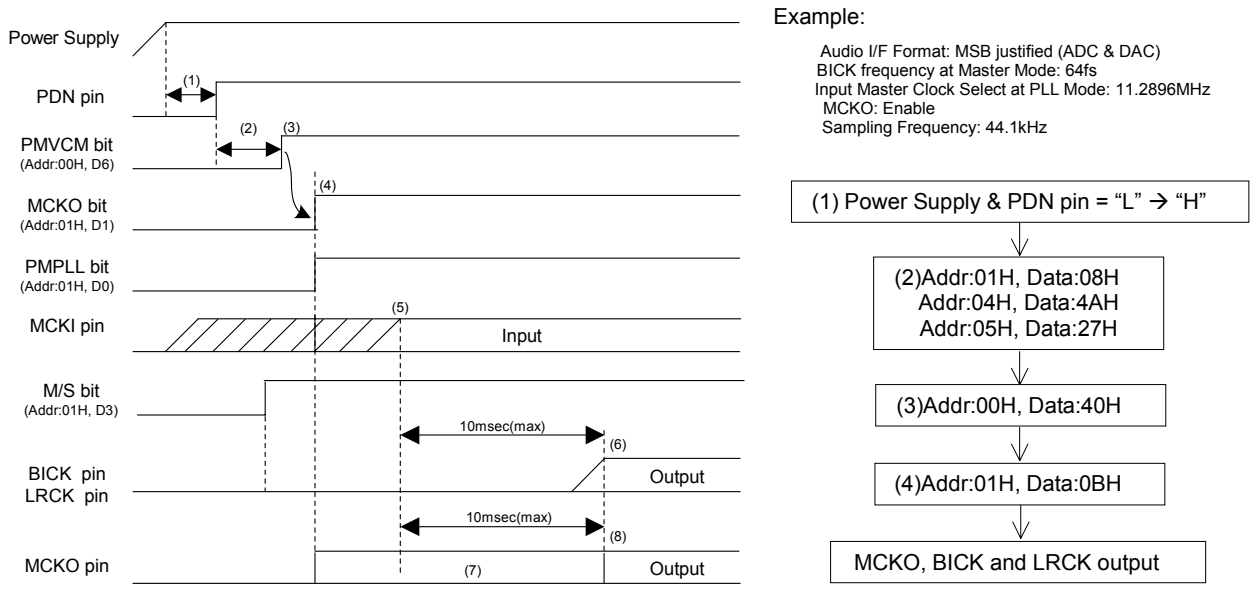


Figure 55. Clock Set Up Sequence (1)

<Example>

(1) After Power Up, PDN pin = "L" → "H"
"L" time of 150ns or more is needed to reset the AK4649VN.
(2) DIF1-0, PLL3-0, FS3-0, BCKO and M/S bits must be set during this period.
(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM must first be powered-up before the other block operates.
(4) In case of using MCKO output: MCKO bit = "1"
In case of not using MCKO output: MCKO bit = "0"
(5) PLL starts after PMPLL bit changes from "0" to "1" and MCKI is supplied from an external source, and PLL lock time is 10ms (max).
(6) The AK4649VN starts to output the LRCK and BICK clocks after the PLL became stable. Then normal operation starts.
(7) The invalid frequency is output from the MCKO pin during this period if MCKO bit = "1".
(8) The normal clock is output from the MCKO pin after the PLL is locked if MCKO bit = "1".

2. PLL Slave Mode (LRCK or BICK pin)

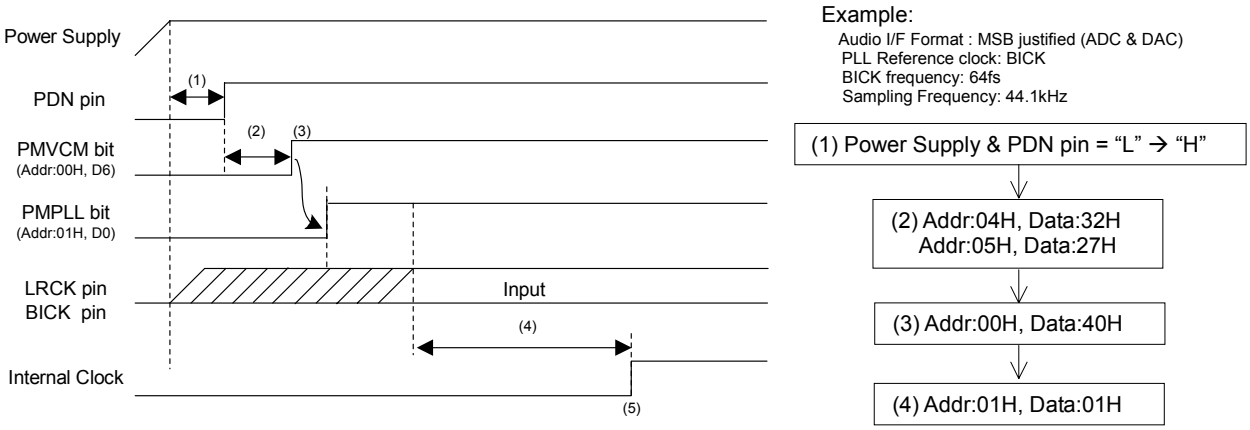


Figure 56. Clock Set Up Sequence (2)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 150ns or more is needed to reset the AK4649VN.

(2) DIF1-0, FS3-0 and PLL3-0 bits must be set during this period.

(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM must first be powered up before the other block operates.

(4) PLL starts after the PMPLL bit changes from "0" to "1" and PLL reference clock (LRCK or BICK pin) is supplied. PLL lock time is 160ms (max) when LRCK is a PLL reference clock. And PLL lock time is 2ms (max) when BICK is a PLL reference clock.

(5) Normal operation stats after that the PLL is locked.

3. PLL Slave Mode (MCKI pin)

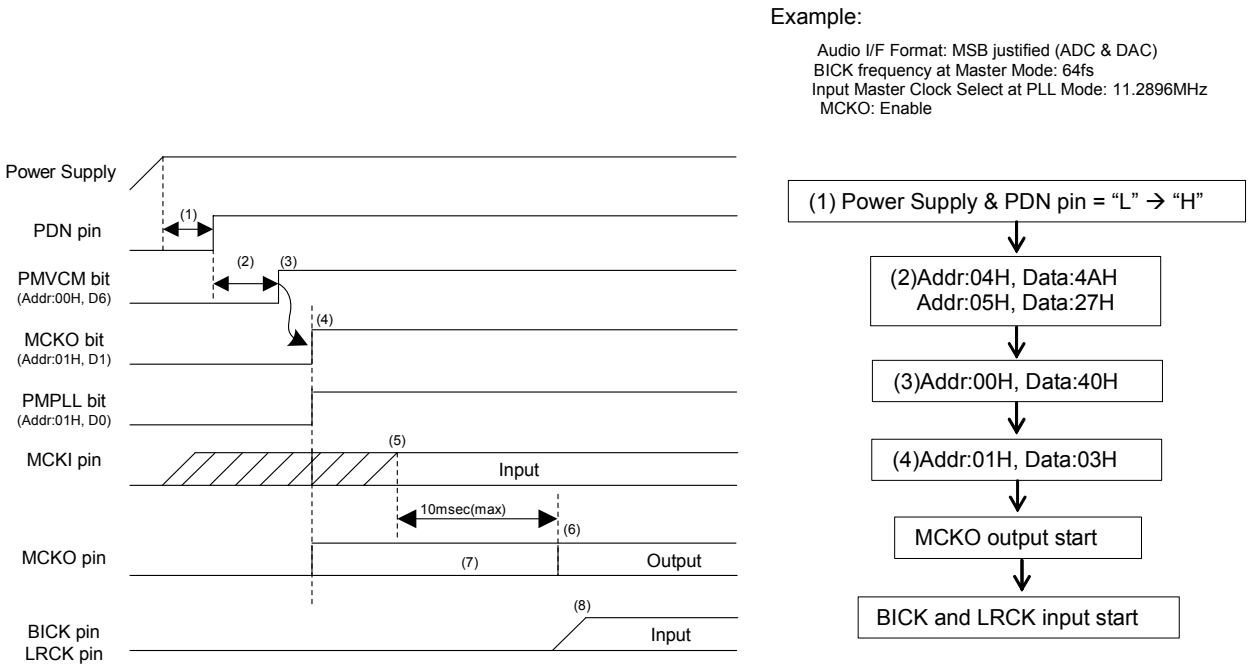


Figure 57. Clock Set Up Sequence (3)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 150ns or more is needed to reset the AK4649VN.
(2) DIF1-0, PLL3-0, FS3-0, BCKO and M/S bits must be set during this period.
(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM must first be powered up before the other block operates.
(4) Enable MCKO output: MCKO bit = "1"
(5) PLL starts after that the PMPLL bit changes from "0" to "1" and PLL reference clock (MCKI pin) is supplied.
PLL lock time is 10ms (max).
(6) The normal clock is output from MCKO after PLL is locked.
(7) The invalid frequency is output from MCKO during this period.
(8) BICK and LRCK clocks must be synchronized with MCKO clock.

4. EXT Slave Mode

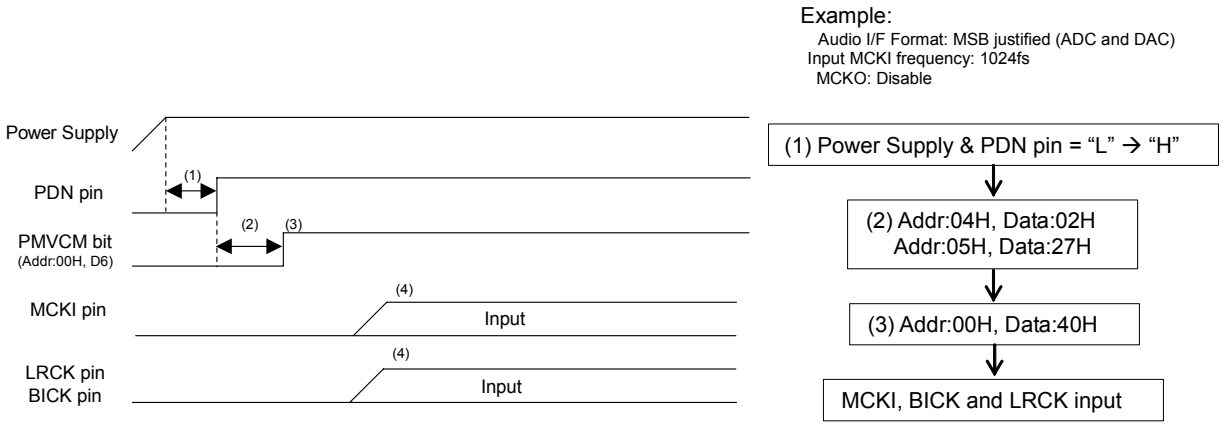


Figure 58. Clock Set Up Sequence (4)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 150ns or more is needed to reset the AK4649VN.

(2) DIF1-0 and FS1-0 bits must be set during this period.

(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM must first be powered up before the other block operates.

(4) Normal operation starts after the MCKI, LRCK and BICK are supplied.

■ MIC Input Recording (Stereo)

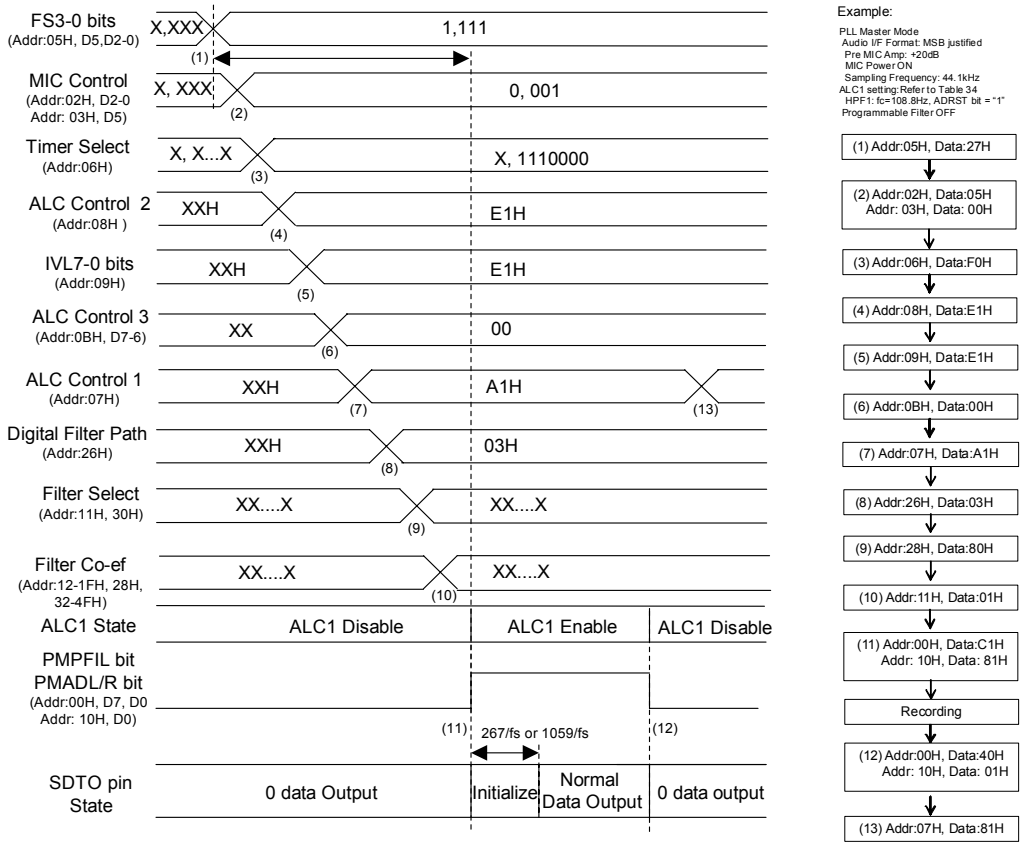


Figure 59. MIC Input Recording Sequence

<Example>

This sequence is an example of ALC1 setting at fs=44.1kHz. For changing the parameter of ALC, please refer to "Figure 36. Registers Set-up Sequence at ALC1 Operation (recording path)"

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS3-0 bits). When the AK4649VN is PLL mode, MIC, ADC and Programmable Filter must be powered-up in consideration of PLL lock time after a sampling frequency is changed.
(2) Set up MIC Gain (Addr = 02H, 03H)
(3) Set up ALC1 Timer and ADRST bit (Addr = 06H)
(4) Set up IREF value for ALC1 (Addr = 08H)
(5) Set up IVOL value at ALC1 operation start
(6) Set up LMTH1 and RGAIN1 bits (Addr = 0BH)
(7) Set up LFST, LMTH0, RGAIN0, LMAT1-0, ZELMN and ALC1 bits (Addr = 07H)
(8) Set up Programmable Filter Path: PFSDO = ADCPF bits = "1" (Addr = 26H)
(9) Set up Coefficient Programmable Filter (Addr = 12H ~ 1FH, 28H, 32H ~ 4FH)
(10) Set up of Programmable Filter ON/OFF
(11) Power Up MIC, ADC and Programmable Filter: PMADL =PMADR =PMPFIL bits = "0" →"1"
The initialization cycle time of ADC is 1059/fs=24ms @ fs=44.1kHz, ADRST bit = "0". ADC outputs "0" data during the initialization cycle. After the ALC1 bit is set to "1", the ALC1 operation starts from IVOL value of (4).
(12) Power Down MIC, ADC and Programmable Filter: PMADL =PMADR =PMPFIL bits = "1" → "0"
(13) ALC1 Disable: ALC1 bit = "1" → "0"

■ Digital MIC Input Recording (Stereo)

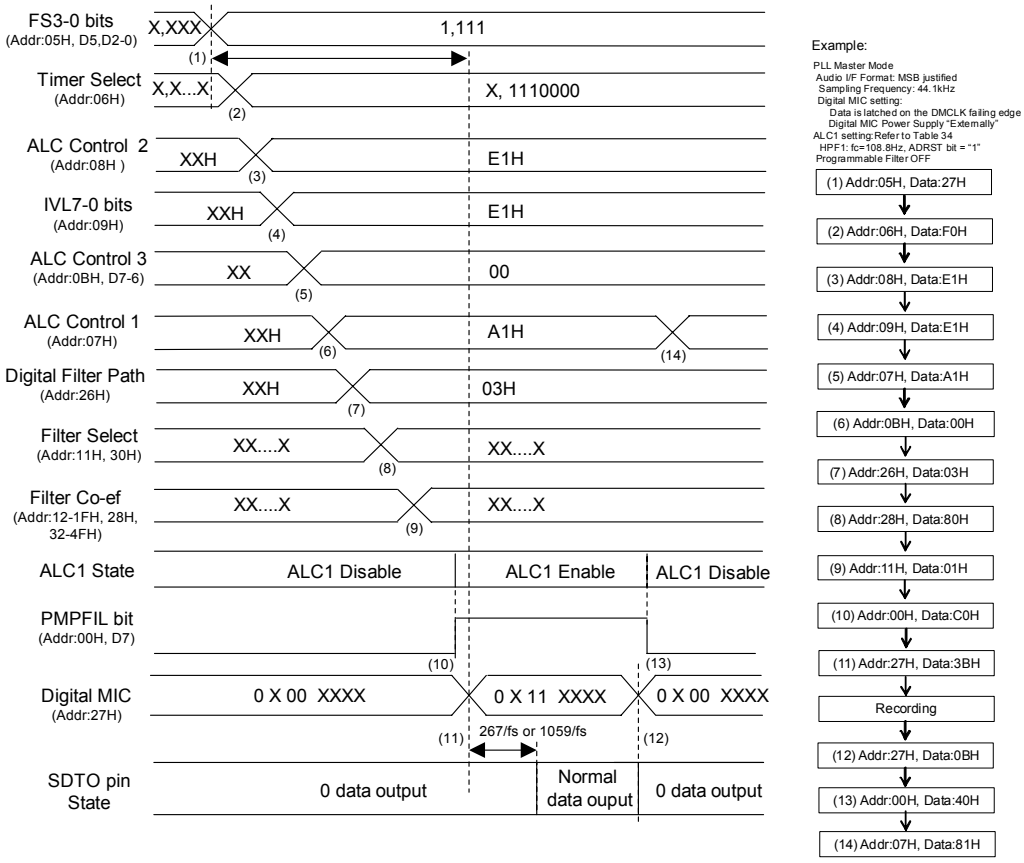


Figure 60. Digital MIC Input Recording Sequence

<Example>

This sequence is an example of ALC1 setting at fs=44.1kHz. For changing the parameter of ALC, please refer to "Figure 36. Registers Set-up Sequence at ALC1 Operation (recording path)"

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS3-0 bits). When the AK4649VN is PLL mode, Digital MIC and Programmable Filter must be powered-up in consideration of PLL lock time after a sampling frequency is changed.
(2) Set up ALC1 Timer and ADRST bit (Addr = 06H)
(3) Set up IREF value for ALC1 (Addr = 08H)
(4) Set up IVOL value at ALC1 operation start (Addr = 09H)
(5) Set up LMTH1 and RGAIN1 bits (Addr = 0BH)
(6) Set up LFST, LMTH0, RGAIN0, LMAT1-0, ZELMN and ALC1 bits (Addr = 07H)
(7) Set up Programmable Filter Path: PFSDO = ADCPF bits = "1" (Addr = 26H)
(8) Set up Coefficient of Programmable Filter (Addr = 12H ~ 1FH, 28H, 32H ~ 4FH)
(9) Set up Programmable Filter ON/OFF
(10) Power Up Programmable Filter: PMPFIL bit = "0" →"1"
(11) Set up & Power Up Digital MIC: PMDMR = PMDML bits = "0" →"1"
The initialization cycle time of ADC is 1059/fs=24ms @ fs=44.1kHz, .ADRST bit = "1". ADC outputs "0" data during initialization cycle. After the ALC1 bit is set to "1", the ALC1 operation starts from IVOL value of (4).
(12) Power Down Digital MIC: PMDMR = PMDML bits = "1" →"0"
(13) Power Down Programmable Filter: PMPFIL bit = "1" → "0"
(14) ALC1 Disable: ALC1 bit = "1" → "0"

■ Speaker-amp Output

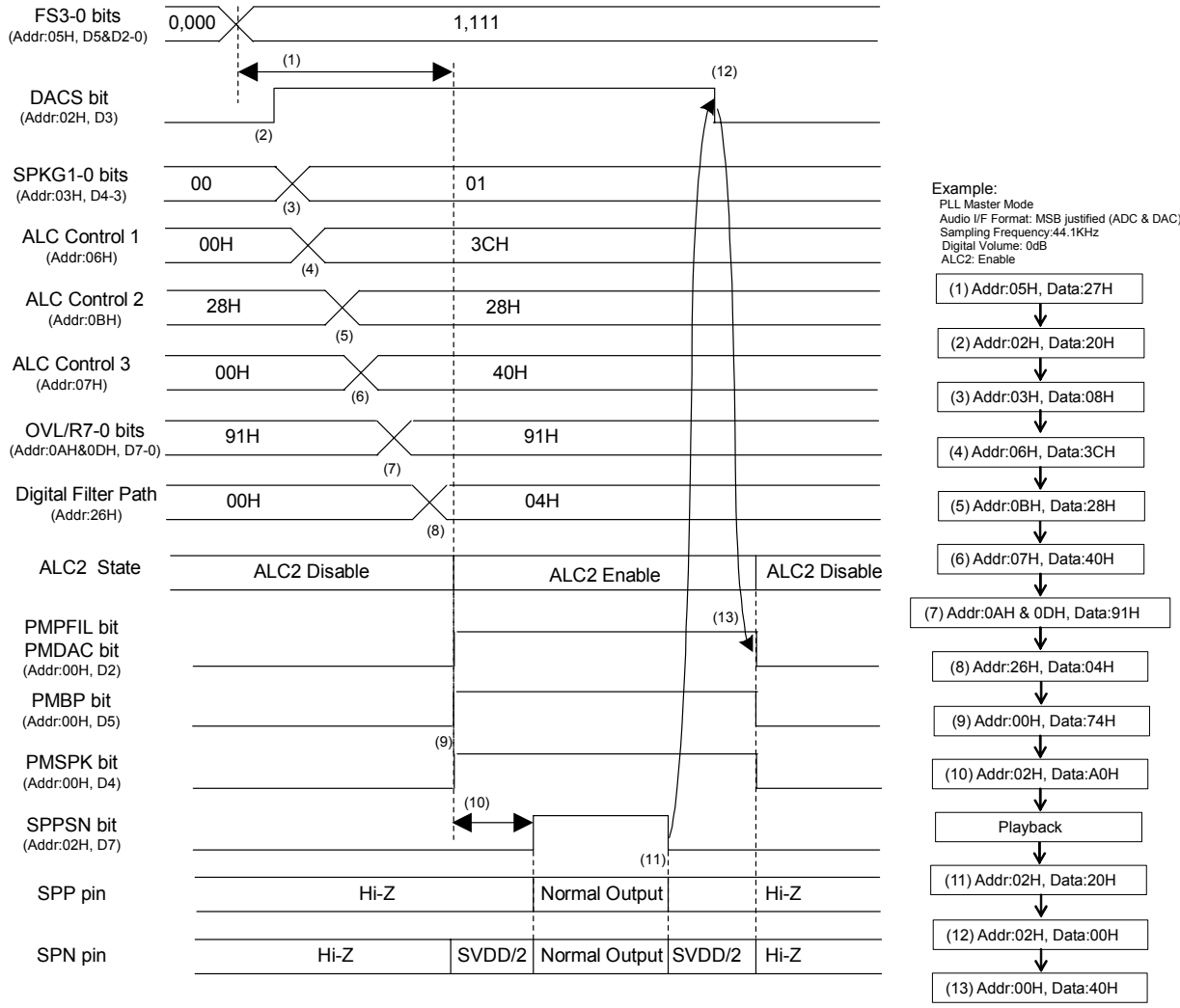


Figure 61. Speaker-Amp Output Sequence

<Example>

At first, clocks must be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS3-0 bits). When the AK4649VN is PLL mode, DAC and Speaker-Amp must be powered-up in consideration of PLL lock time after a sampling frequency is changed.

(2) Set up the path of "DAC → SPK-Amp": DACS bit = "0" → "1"

(3) SPK-Amp gain setting: SPKG1-0 bits = "00" → "01"

(4) Set up Timer Select for ALC (Addr = 06H)

(5) Set up REF value for ALC, LMTH1 and RGAIN1 bits (Addr = 0BH)

(6) Set up LMTH0, RGAIN0, LMAT1-0, ALC2 bits (Addr = 07H)

(7) Set up the output digital volume (Addr = 0AH, 0DH).
When OVOLC bit is "1" (default), OVL7-0 bits set the volume of both channels. After DAC is powered-up, the digital volume changes from default value (0dB) to the register setting value by the soft transition. When ALC2 bit = "0", it could be digital volume control.

(8) Set up Programmable Filter Path (PFDAC, ADCPF and PFSDO bits) (Addr = 26H)

(9) Power up DAC, MIN-Amp, Programmable Filter and Speaker:
PMDAC = PMPFIL = PMBP = PMSPK bits = "0" → "1"

(10) Exit the power-save-mode of Speaker-Amp: SPPSN bit = "0" → "1"
"(9)" time depends on the time constant of external resistor and capacitor connected to the MIN pin. If Speaker-Amp output is enabled before input of MIN-Amp becomes stable, pop noise may occur.
e.g. R=33kΩ, C=0.1μF: Recommended wait time is more than 5τ = 16.5ms.
(11) Enter Speaker-Amp Power-save-mode: SPPSN bit = "1" → "0"
(12) Disable the path of "DAC → SPK-Amp": DACS bit = "1" → "0"
(13) Power down DAC, MIN-Amp Programmable Filter and Speaker:
PMDAC = PMPFIL = PMBP = PMSPK bits = "1" → "0"

■Mono Signal Output from Speaker-Amp

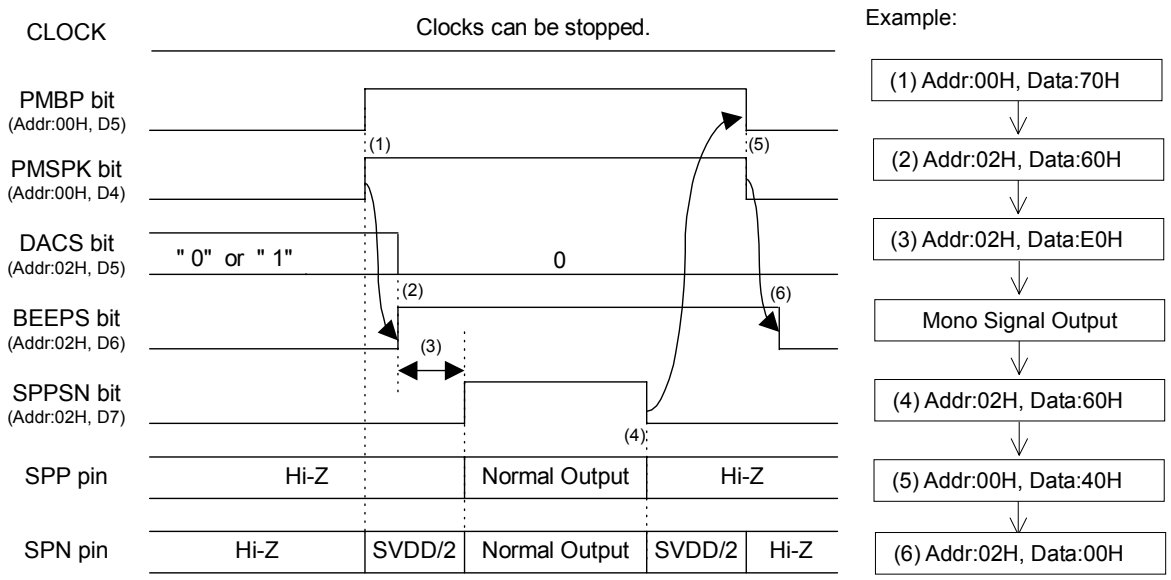


Figure 62. "MIN-Amp → Speaker-Amp" Output Sequence

<Example>
The clocks can be stopped when only MIN-Amp and Speaker-Amp are operating.

(1) Power Up MIN-Amp and Speaker-Amp: PMBP = PMSPK bits = "0" → "1"
(2) Disable the path of "DAC → SPK-Amp": DACS bit = "0"
Enable the path of "MIN → SPK-Amp": BEEPS bit = "0" → "1"
(3) Exit the power-save-mode of Speaker-Amp: SPPSN bit = "0" → "1"
"(3)" time depends on the time constant of external resistor and capacitor connected to MIN pin. If Speaker-Amp output is enabled before input of MIN-Amp becomes stable, pop noise may occur.
e.g. R=33kΩ, C=0.1μF: Recommended wait time is more than 5τ = 16.5ms.
(4) Enter the power-save-mode of Speaker-Amp: SPPSN bit = "1" → "0"
(5) Power Down MIN-Amp and Speaker-Amp: PMBP = PMSPK bits = "1" → "0"
(6) Disable the path of "MIN → SPK-Amp": BEEPS bit = "1" → "0"

■ Stereo Line Output

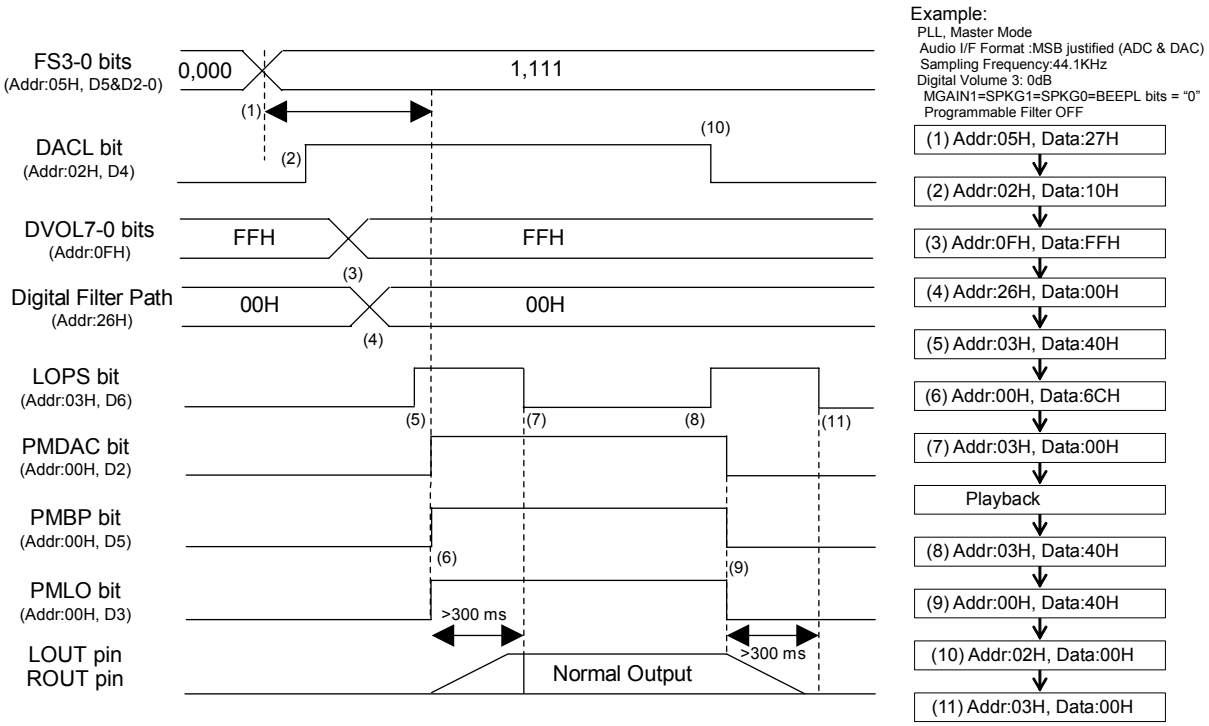


Figure 63. Stereo Lineout Sequence

<Example>

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up the sampling frequency (FS3-0 bits). When the AK4646 is PLL mode, DAC and Stereo Line-Amp must be powered-up in consideration of PLL lock time after the sampling frequency is changed.
(2) Set up the path of "DAC → Stereo Line Amp": DACL bit = "0" → "1"
(3) Set up the output digital volume3 (Addr = 0FH)
(4) Set up the path of Programmable Filter (PFDAC, ADCPF and PFSDO bits) (Addr = 26H)
(5) Enter power-save mode of Stereo Line Amp: LOPS bit = "0" → "1"
(6) Power-up DAC, MIN-Amp and Stereo Line-Amp: PMDAC = PMBP = PMLO bits = "0" → "1"
LOUT and ROUT pins rise up to VCOM voltage after PMLO bit is changed to "1". Rise time to 99% VCOM voltage is 300ms (max) at C=1μF and R_L=10kΩ.
(7) Exit power-save mode of Stereo Line-Amp: LOPS bit = "1" → "0"
LOPS bit must be set to "0" after LOUT and ROUT pins rise up. Stereo Line-Amp goes to normal operation by setting LOPS bit to "0".
(8) Enter power-save mode of Stereo Line-Amp: LOPS bit: "0" → "1"
(9) Power-down DAC, MIN-Amp and Stereo Line-Amp: PMDAC = PMBP = PMLO bits = "1" → "0"
LOUT and ROUT pins fall down to 1% VCOM voltage. Fall time is 300ms (max) at C=1μF and R_L=10kΩ.
(10) Disable the path of "DAC → Stereo Line-Amp": DACL bit = "1" → "0"
(11) Exit power-save mode of Stereo Line-Amp: LOPS bit = "1" → "0"
LOPS bit must be set to "0" after LOUT and ROUT pins fall down.

■ Stop of Clock

Master clock can be stopped when ADC, DAC, Digital MIC and Programmable Filter are not used.

1. PLL Master Mode

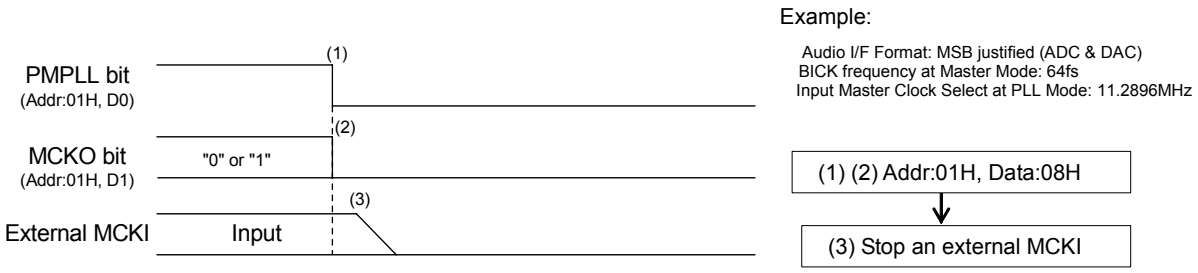


Figure 64. Clock Stopping Sequence (1)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
(2) Stop MCKO clock: MCKO bit = "1" → "0"
(3) Stop an external master clock.

2. PLL Slave Mode (LRCK or BICK pin)

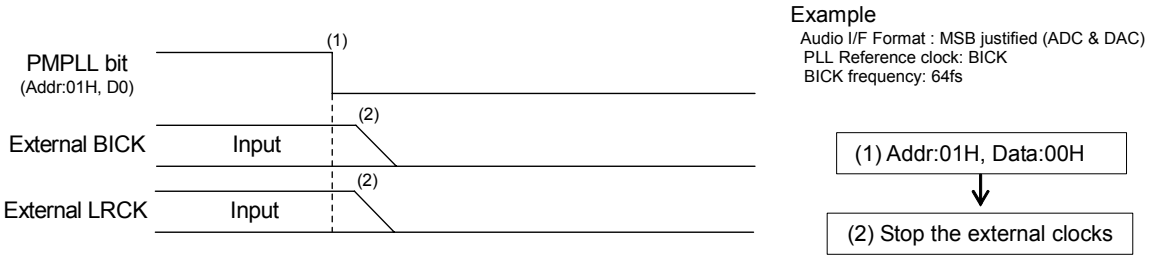


Figure 65. Clock Stopping Sequence (2)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
(2) Stop the external BICK and LRCK clocks

3. PLL Slave (MCKI pin)

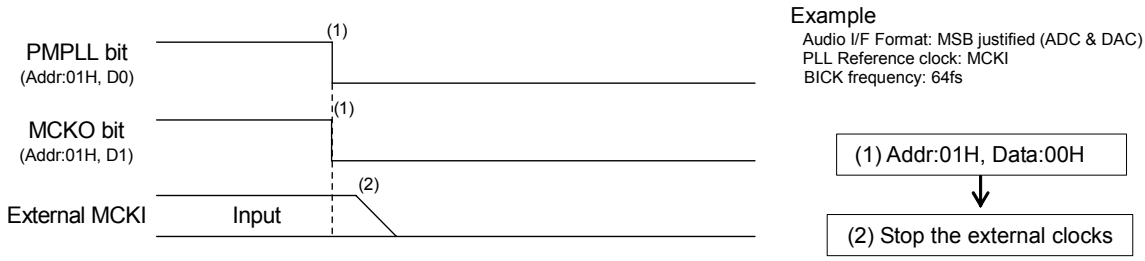


Figure 66. Clock Stopping Sequence (3)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
Stop MCKO output: MCKO bit = "1" → "0"
(2) Stop the external master clock.

4. EXT Slave Mode

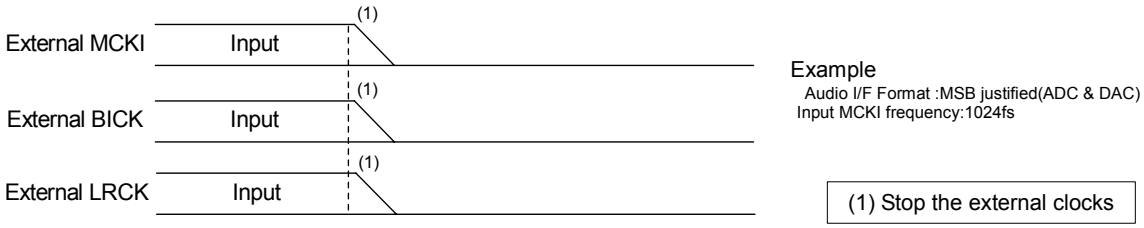


Figure 67. Clock Stopping Sequence (4)

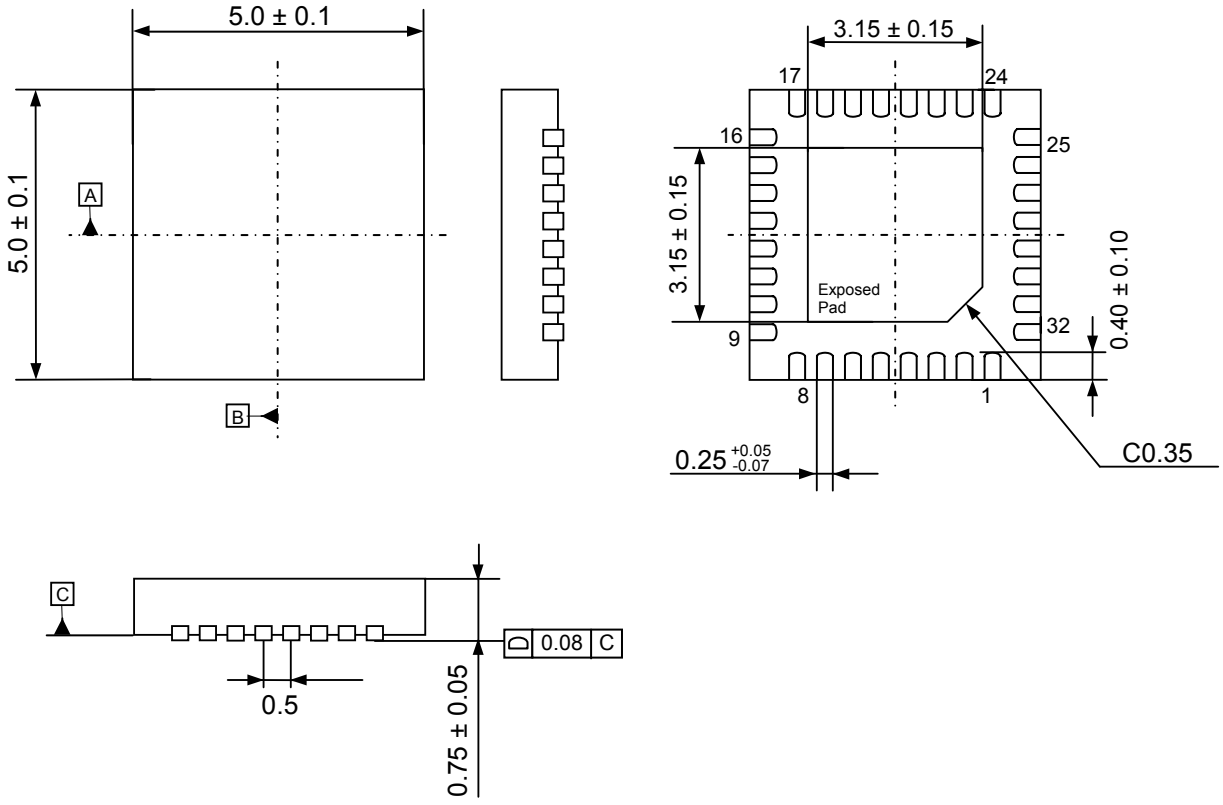
<Example>
(1) Stop the external MCKI, BICK and LRCK clocks.

■ Power down

Power supply current can be shut down (typ. 1μA) by stopping clocks and setting PMVCM bit = "0" after all blocks except for VCOM are powered-down. Power supply current can be also shut down (typ. 1μA) by stopping clocks and setting PDN pin = "L". When PDN pin = "L", the registers are initialized.

PACKAGE (AK4649VN)

32pin QFN (Unit: mm)

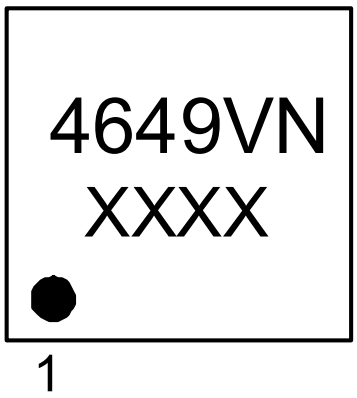


Note: The exposed pad on the bottom surface of the package must be connected to the ground.

■ Material & Lead finish

Package molding compound: Epoxy
Lead frame material: Cu
Inner plating: Ni/Pd/Au-Ag
Outer plating: Ni/Pd/Au

MARKING(AK4649VN)



"4649VN" : Market Number
XXXX : Date code (4 digit)
● : Pin #1 indication

REVISION HISTORY

Date (Y/M/D)	Revision	Reason	Page	Contents
13/01/09	00	First Edition		

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